

CONTENT	SHEET
Cover Sheet, Block diagram	1-2
Intel LGA775 CPU - Signals/ Power/ GND	3-5
Intel Bearlake - FSB, PCIE, DMI, VGA, MSIC	6
Intel Bearlake - Memory DDR2	7
Intel Bearlake - Power / GND	8-9
ICH9 - PCI, USB, DMI, PCIE	10
ICH9 - Host, DMI, SATA, Audio, SPI, RTC, MSIC	11
ICH9 - Power, GND	12
DDR2 Chanel-A / Chanel-B	13-14
Clock Gen ICS9LPRS900	15
Super I/O Fintek F71882	16
PS2 / COM / VGA Port	17
SATA / FAN Control	18
LAN Realtek RTL8111(PCIE)	19
Audio Codec ALC888	20
PCIE x16,x1	21
PCI Slot 1 & 2	22
Marvell 88SE6111 PCIE to IDE/ SATA	23
USB Connectors	24
IEEE1394 VT6308	25
System Power/ACPI Controller UPI	26
DDR2 / NB-Core Switching Power	27
VRD 11 - ISL6322 (3 Phases)	28
ATX Power-Con. / F_Panel	29
Manual & Option Parts	30
Power Delivery	31
Reset & PWROK map	32
GPIO Setting & PCI Routing / Revision History	33-34

MS-7360

ATX Version: 0A

CPU: Intel Pentium 4, Pentium D, Core2 Duo, Wolfdale, Kentsfield and Yorkfield processors in LGA775 Package.

System Chipset:

Intel Bearlake - Q/G/P (G33, P35, Q35/33North Bridge)
Intel ICH9 (South Bridge)

On Board Device:

CLOCK Gen -- ICS 9LPRS900
LPC Super I/O -- Fintek F71882F
LAN -- Realtek 8111 (PCIE)
HD Audio Codec -- ALC888
1394 Controller -- VT6307 / VT6308 (2-port)
PCIE to PATA/SATA Bridge -- Marvel 88SE6111

Main Memory:

Dual-channel DDR-II * 4

Expansion Slots:

PCI EXPRESS X16 SLOT *3
PCI SLOT * 2

PWM: Intersil ISL6322 (3 Phases) w/ ISL6612 driver

Configuration and BOM match up

Option	Function	Orcad Configure	BOM
STD	Bearlake-G/ICH9/ICH-Fan/Non-PCIEx4	cfg-STD	601-72345-A10

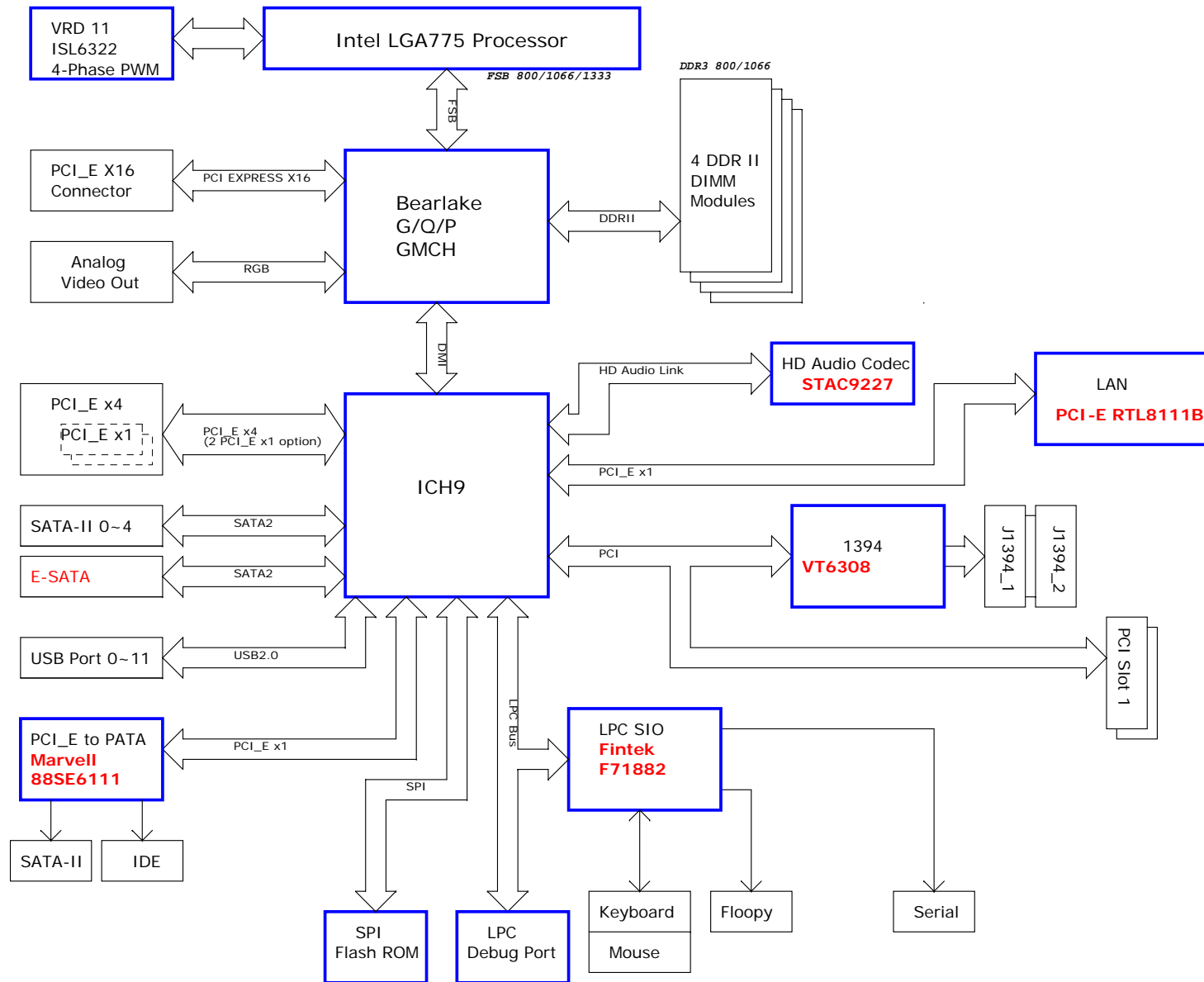


MICRO-STAR INT'L CO.,LTD

MS-7360

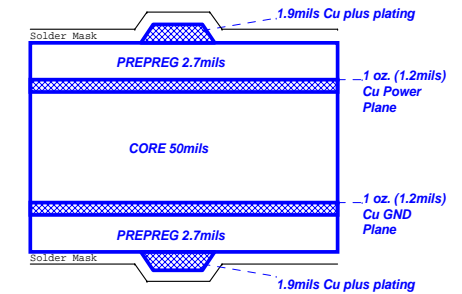
Size Custom	Document Description COVER SHEET	Rev 1.0
Date: Monday, March 05, 2007	Sheet 1 of 34	

Block Diagram



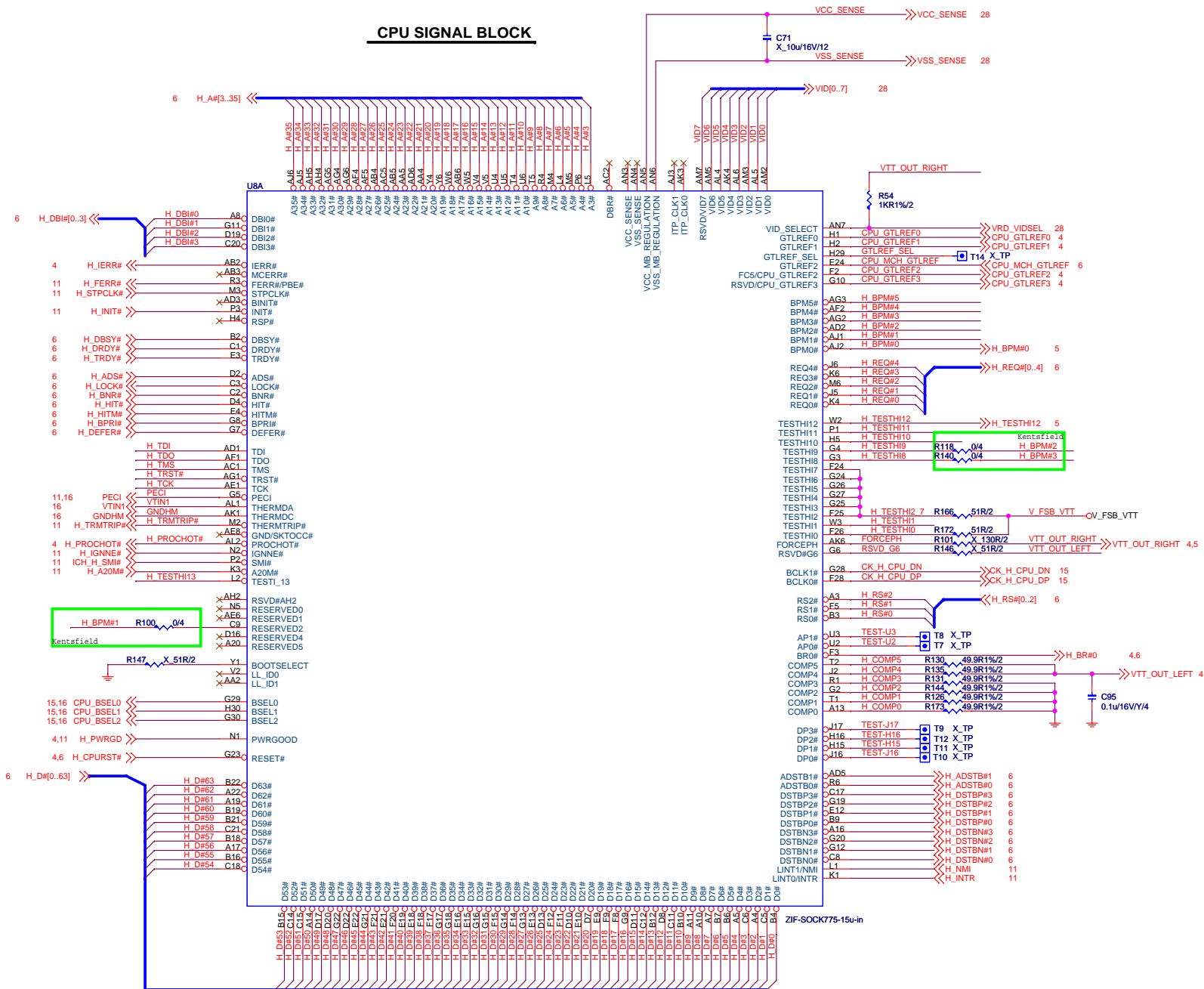
Board Stack-up

(1080 Prepreg Considerations)

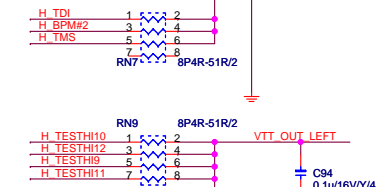
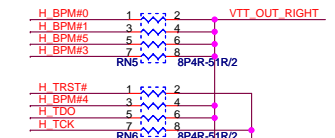
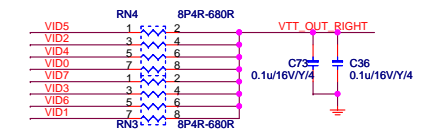


Single End 50ohm Top/Bottom : 4mils
 USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
 SATA - 95ohm : 15/4/8/4/15
 LAN - 100ohm : 15/4/8/4/15
 PCIE - 95ohm : 15/4/8/4/15
 IEEE1394 - 110ohm : 15/4/9/4/15
 IDE : 15/4/8/4/15

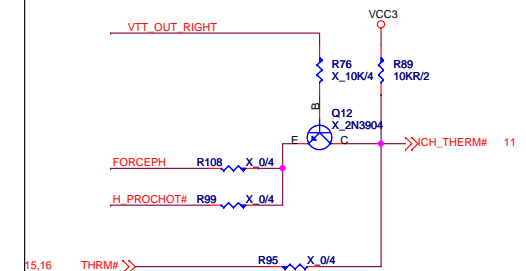
CPU SIGNAL BLOCK



PULL HIGHT PULL DOWN



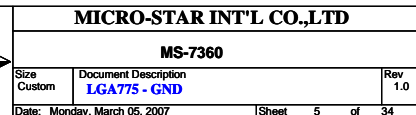
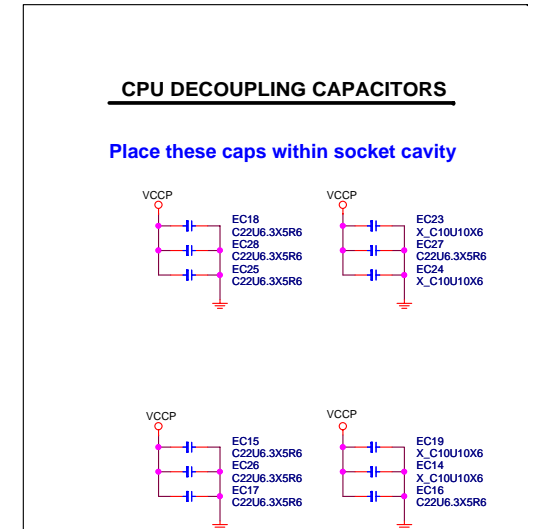
Thermal TRIP

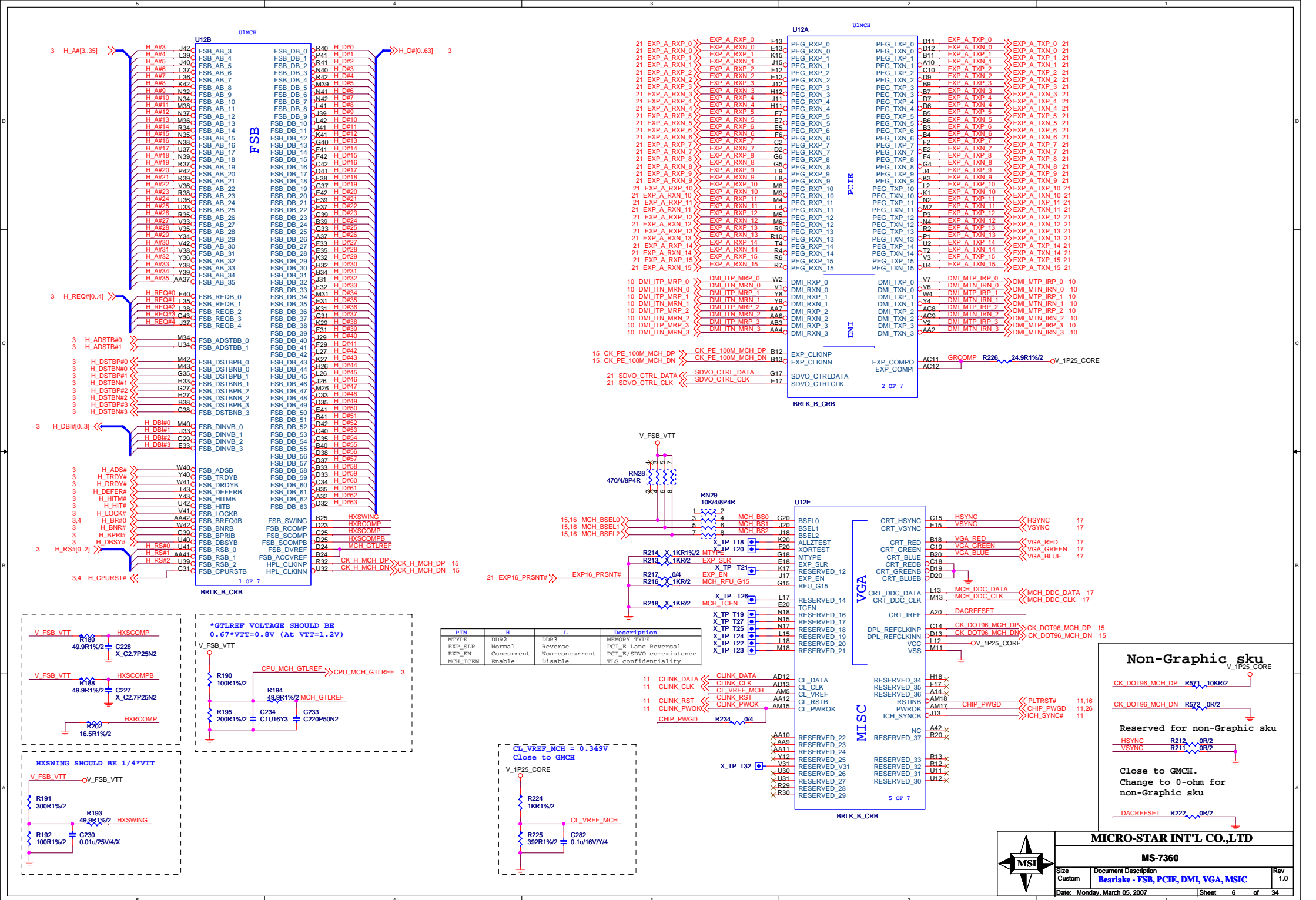


MICRO-STAR INT'L CO.,LTD

MS-7360

Size Custom	Document Description LGA775 - Signal	Rev 1.0
Date: Monday, March 05, 2007		Sheet 3 of 34



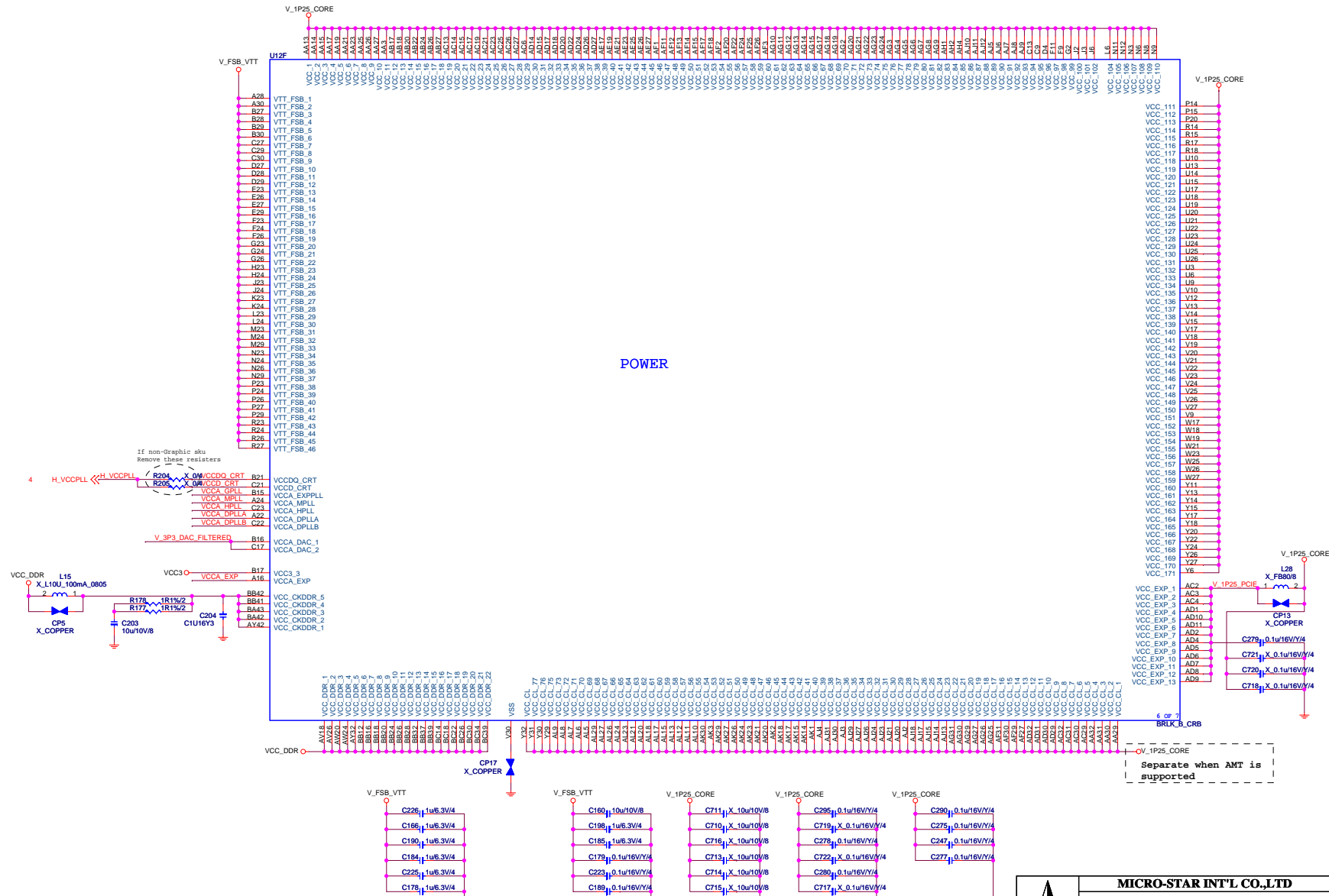
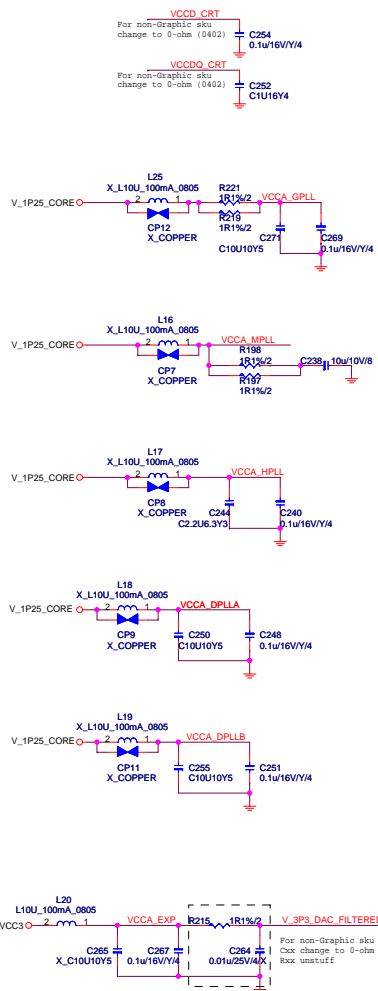


MICRO-STAR INT'L CO.,LTD

MS-7360

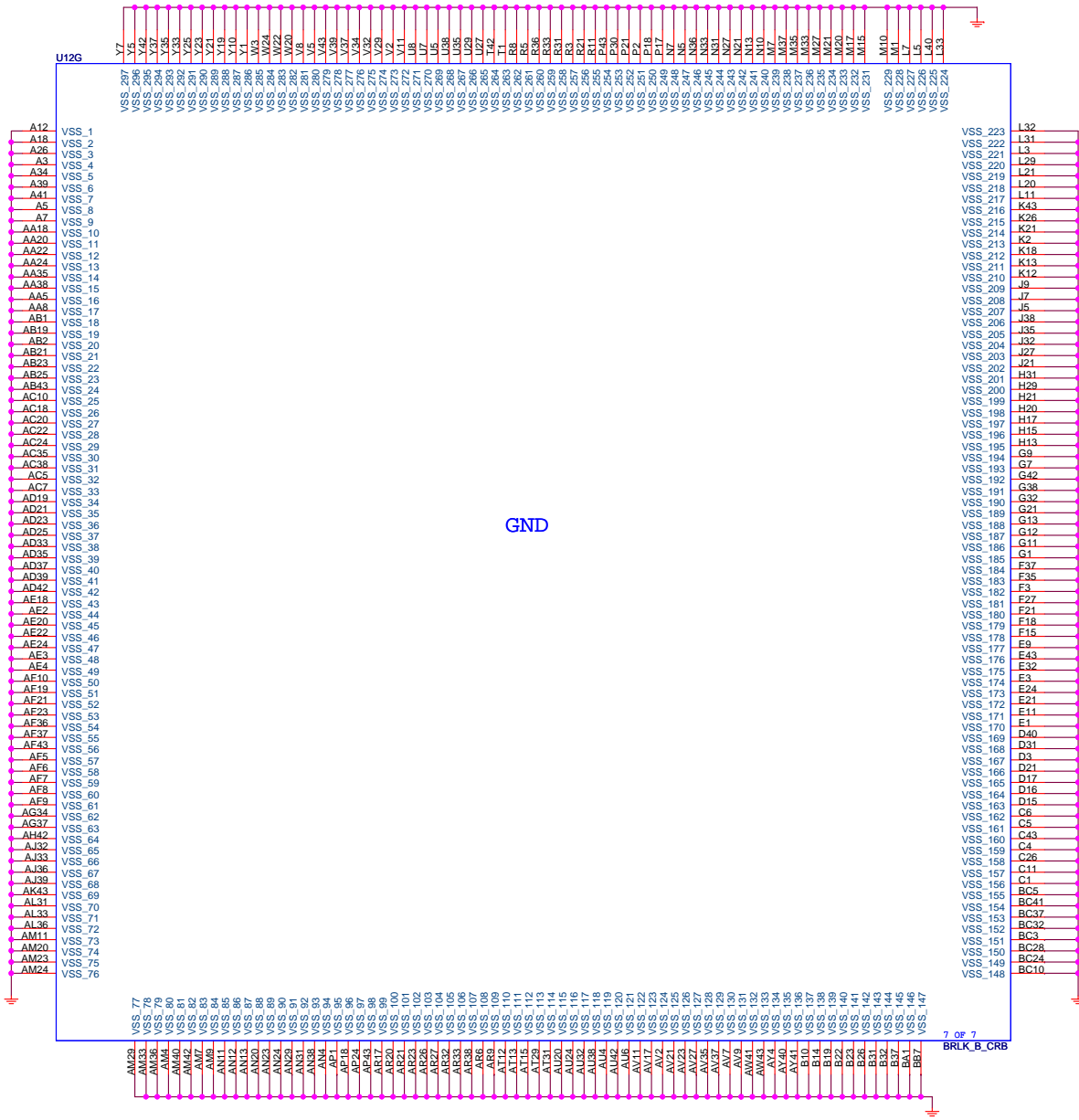
Size Custom	Document Description Bearlake - FSB, PCIE, DMI, VGA, MSIC	Rev 1.0
Date: Monday, March 05, 2007		Sheet 6 of 34

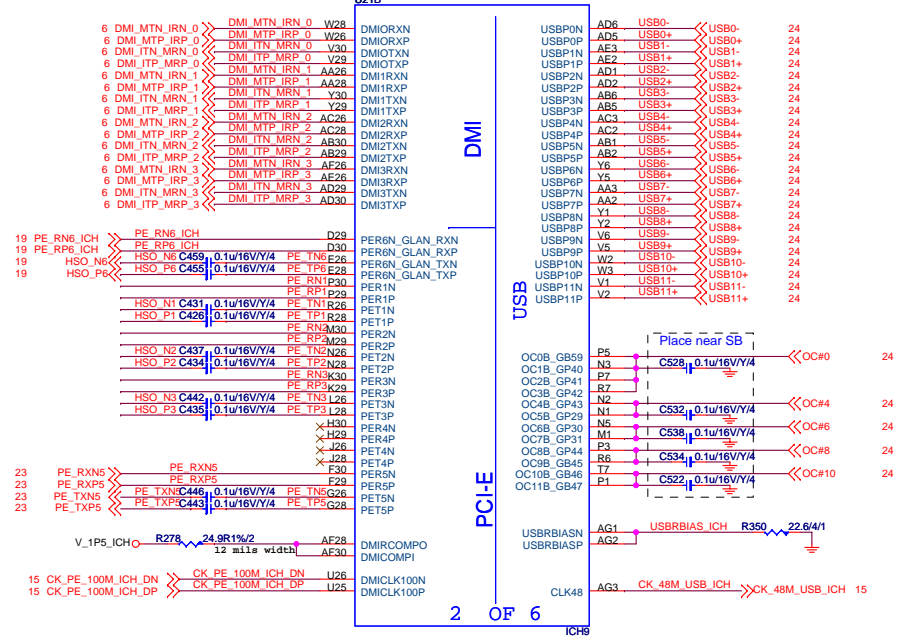
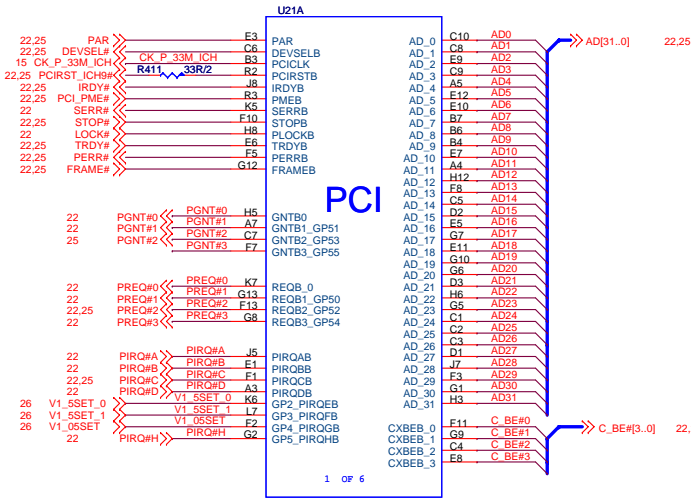
NB POWER



MICRO-STAR INT'L CO.,LTD

Size Custom	Document Description Bearlake - Power	Rev 1.0
Date: Monday, March 05, 2007		Sheet 8 of 34





SB STRAPPING RESISTOR

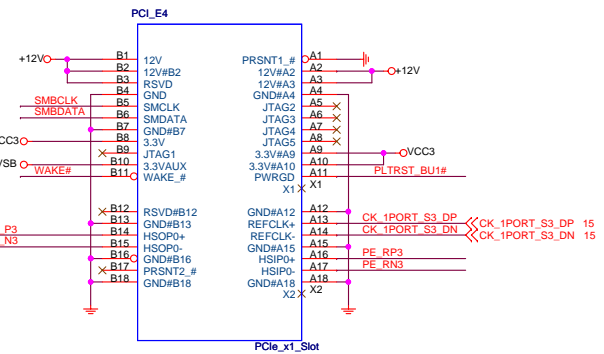
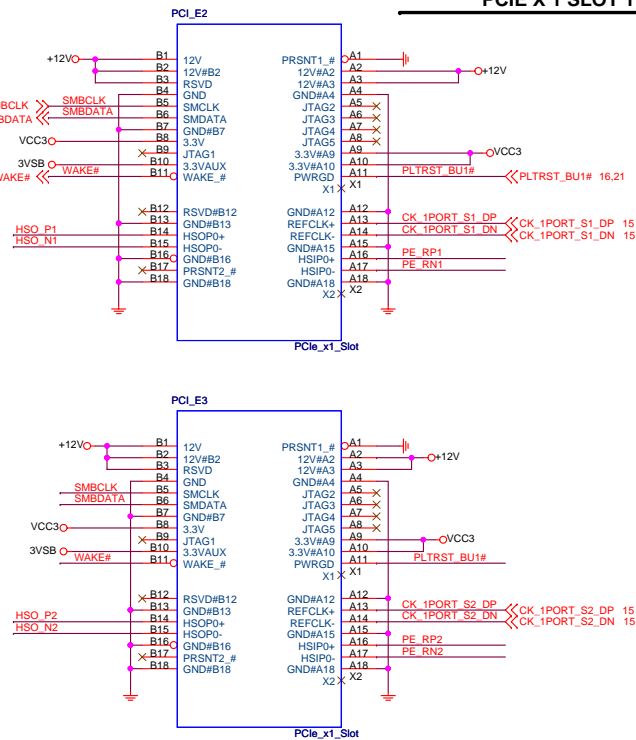


BOOT SELECT STRAPS			
BOOT DEVICE	GNT#0	SPI_CS1#	
FWH	1	1	
SPI	0	1	
PCI	1	0	



SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERRIDE
GNT2	N/A	SET BIT	PCI PORT CONFIG 2 BIT 0 (5-6)

PCIEX1 SLOT 1,2,3



MICRO-STAR INT'L CO.,LTD

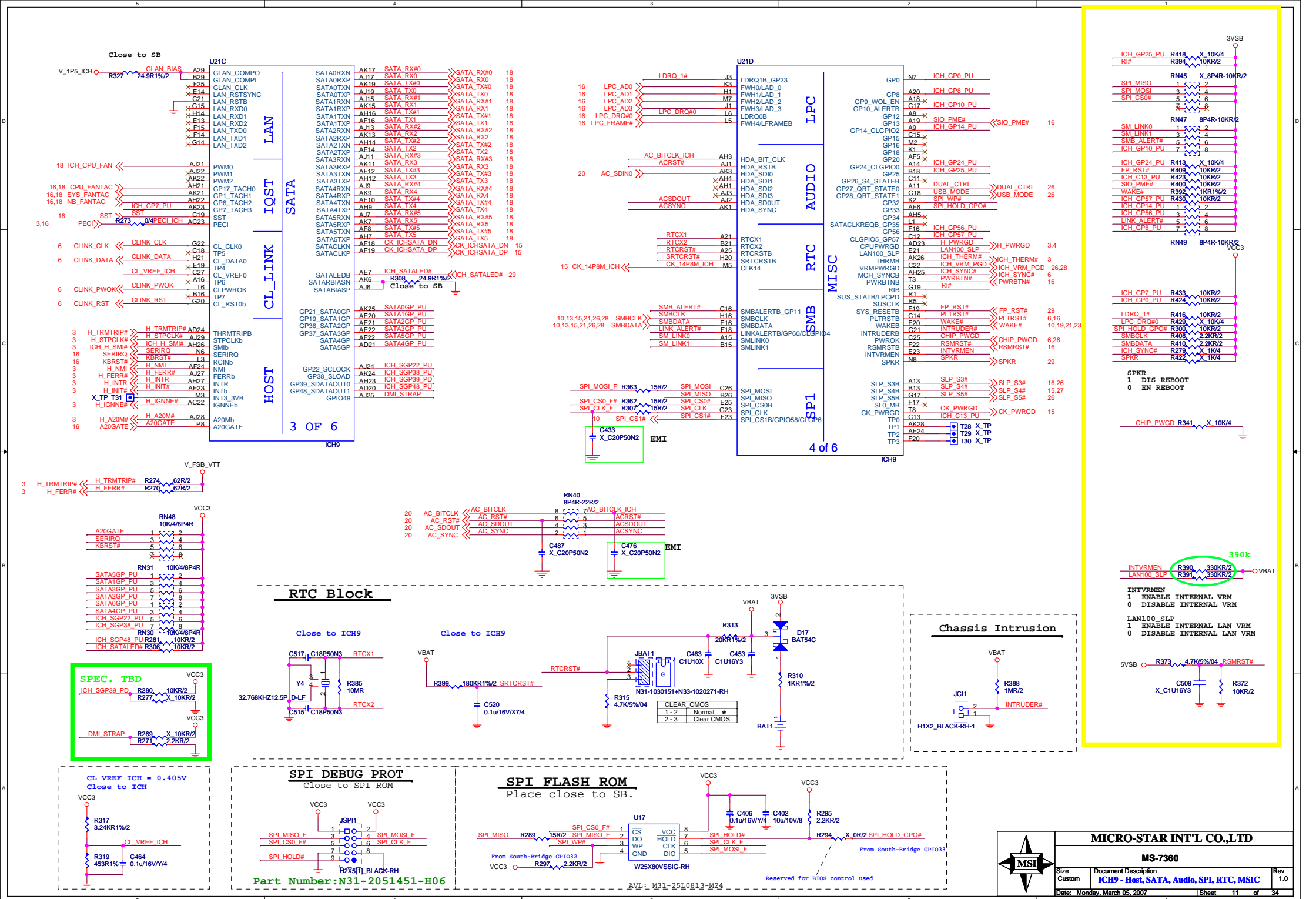
MS-7360

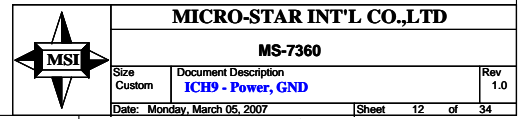
Size Custom Document Description **IC99 - PCI, DMI, USB, PCIE & Slots**

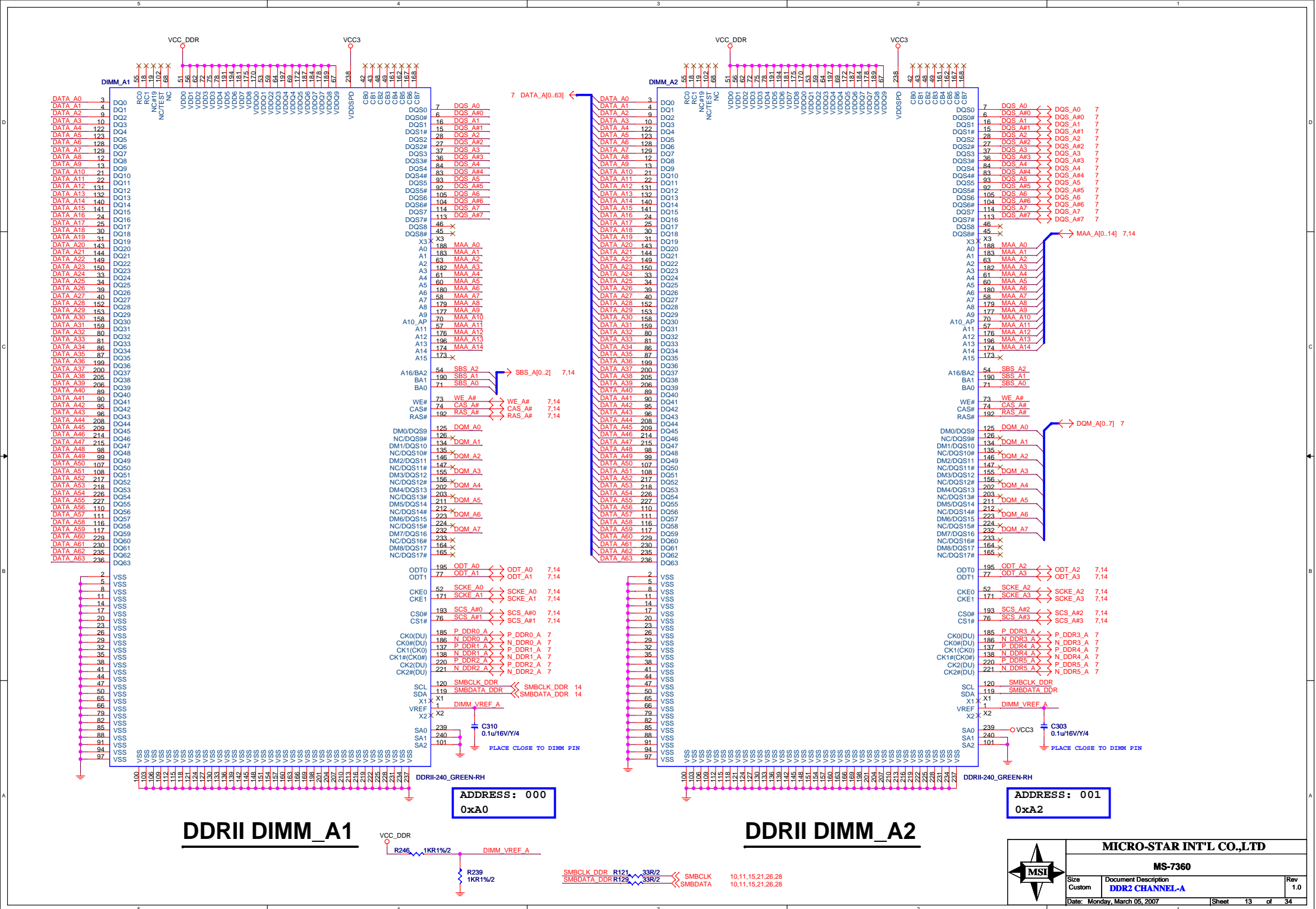
Rev 1.0

Date: Monday, March 05, 2007

Sheet 10 of 34



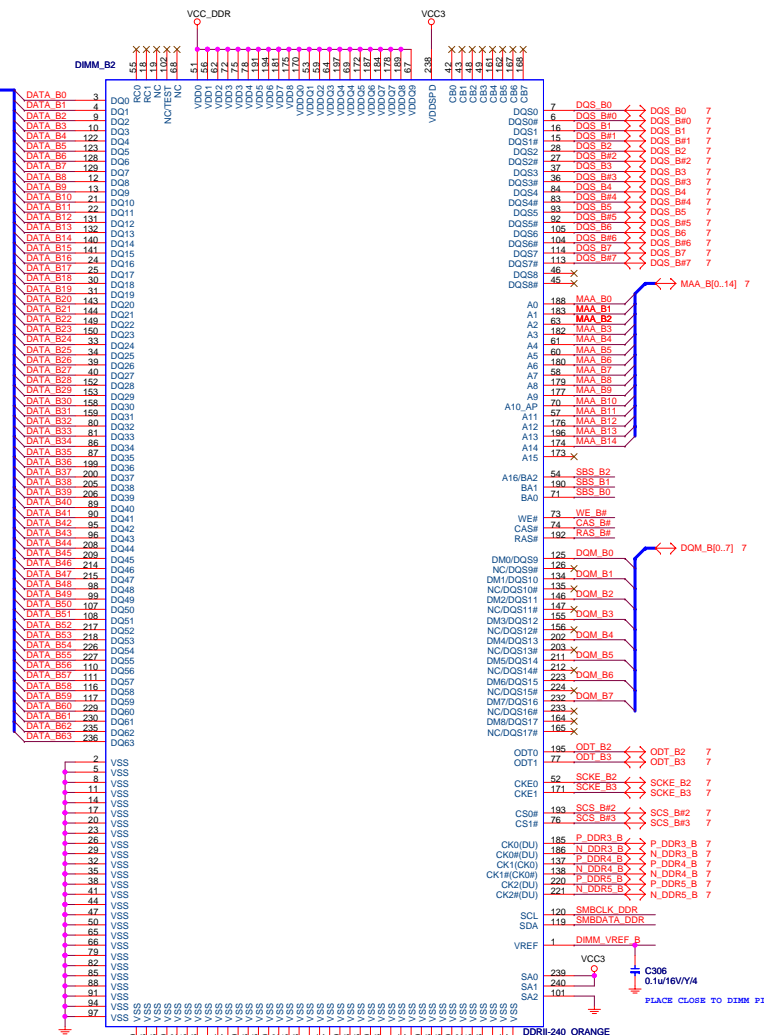




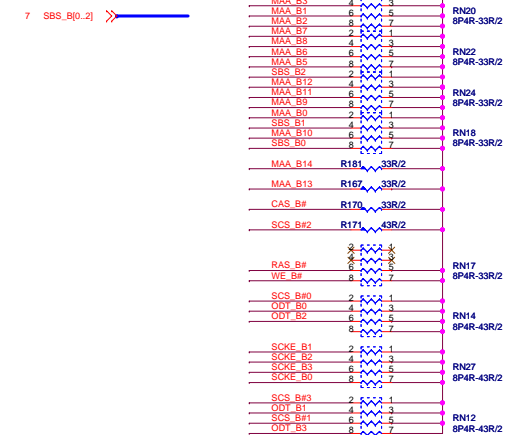
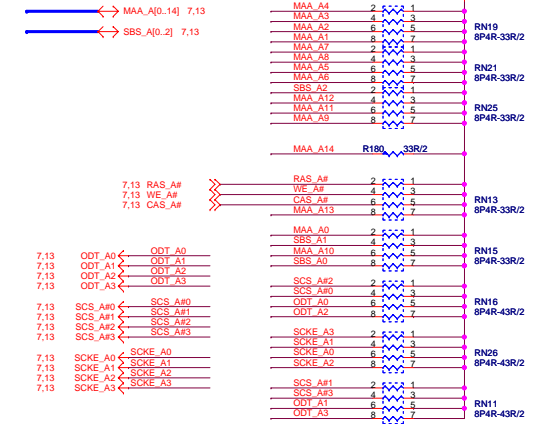
DDR II Termination

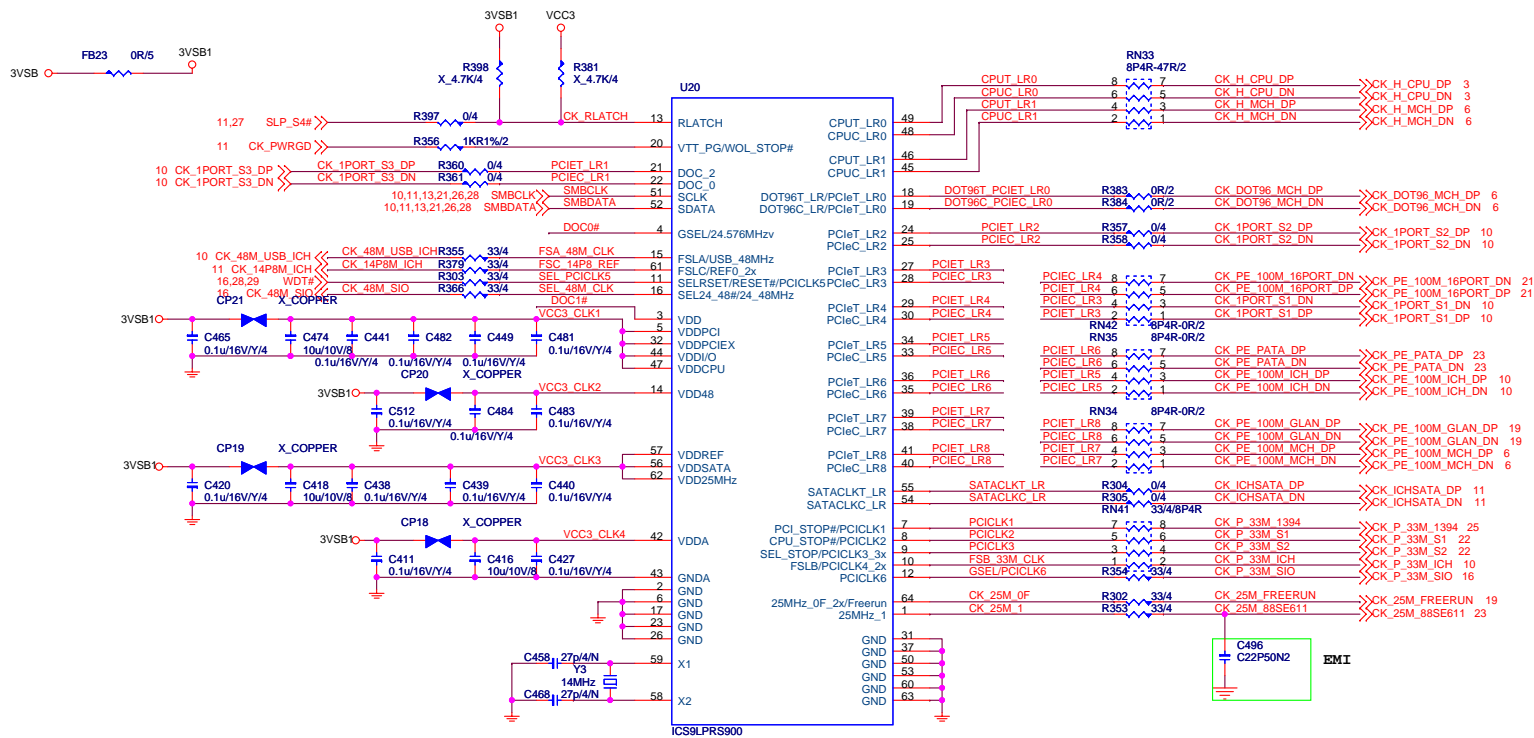


DDR II DIMM B1

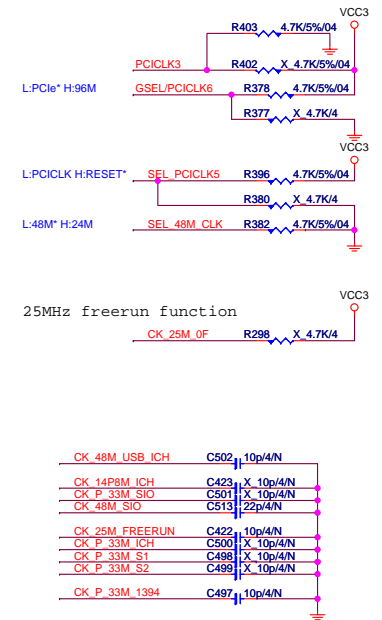


DDR II DIMM B2



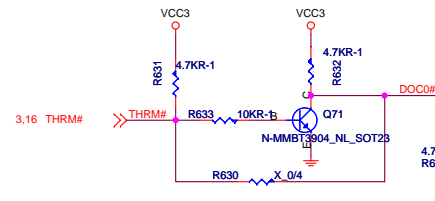
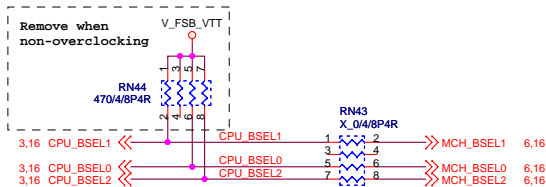


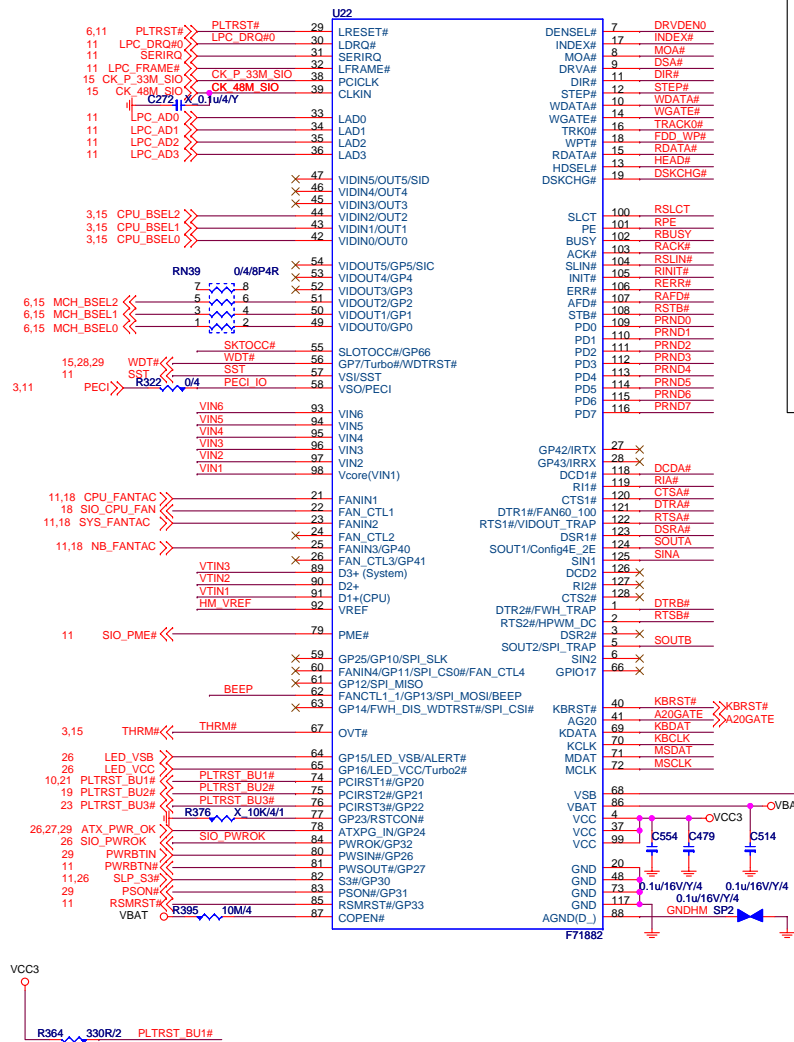
CLOCK GEN STRAPPING



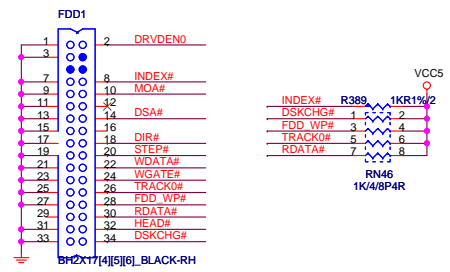
BSEL	TABLE
2 1 0	FSB FREQUENCY
0 0 0	266 MHz (1066)
0 0 1	133 MHz (533)
0 1 0	200 MHz (800)

CPU_BSEL0 R351 1KR1%/2 FSA 48M CLK
CPU_BSEL1 R352 1KR1%/2 FSB 33M CLK
CPU_BSEL2 R296 1KR1%/2 FSC 14P8 REF

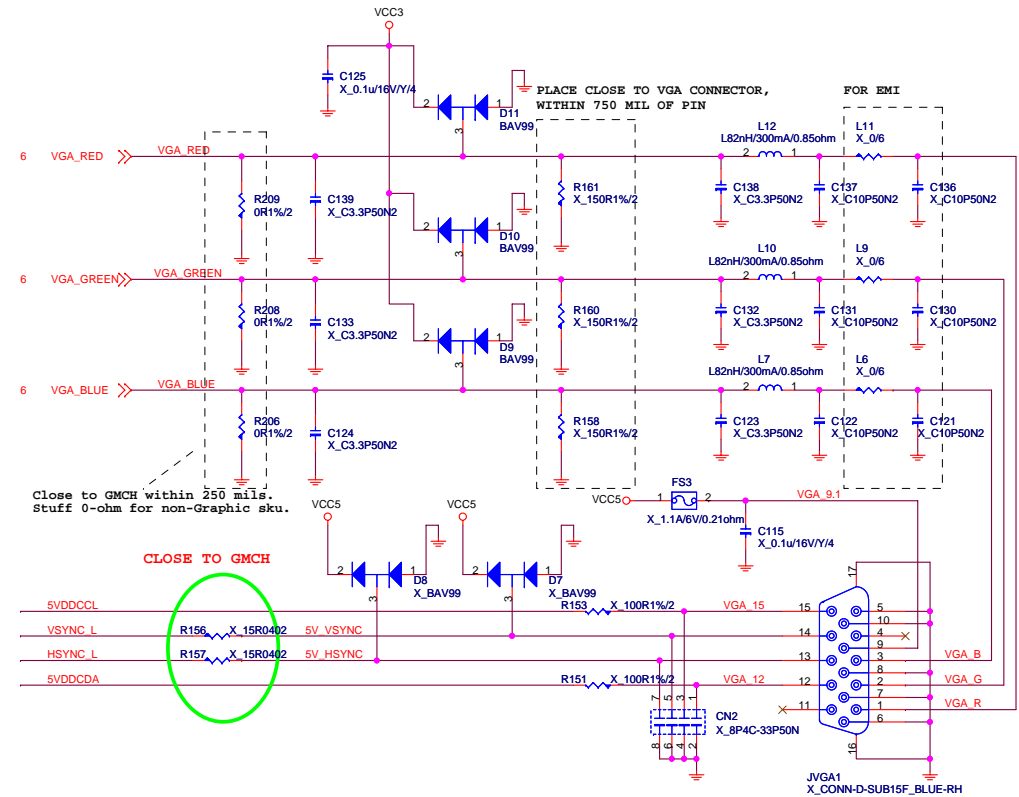
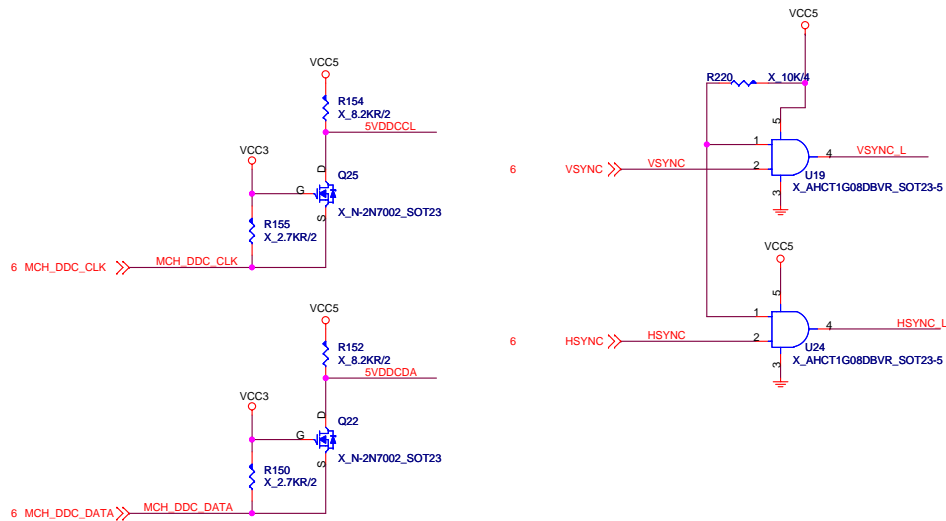




FLOPPY CONNECTOR



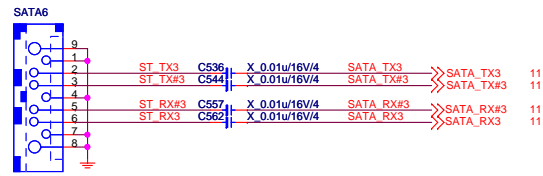
Video Connector



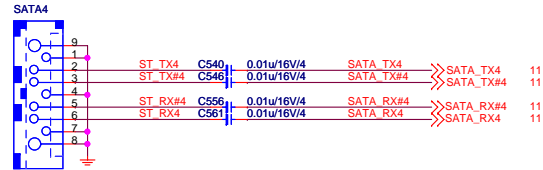
MICRO-STAR INT'L CO.,LTD

MS-7360

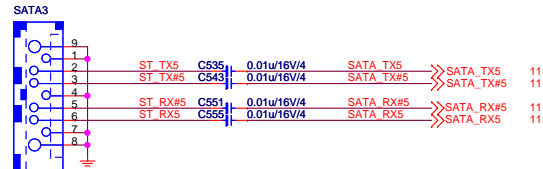
Size Custom	Document Description VGA	Rev 1.0
Date: Monday, March 05, 2007		Sheet 17 of 34



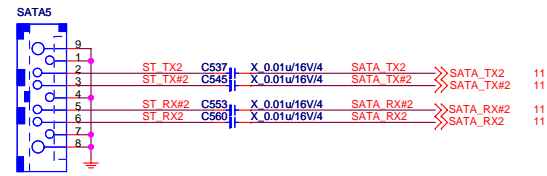
X_CONN-SATA10P_PURPLE



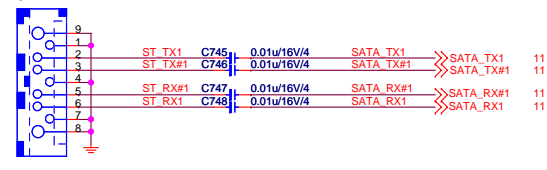
CONN-SATA10P_PURPLE



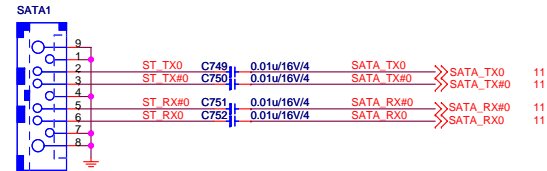
CONN-SATA10P_PURPLE



X_CONN-SATA10P_PURPLE

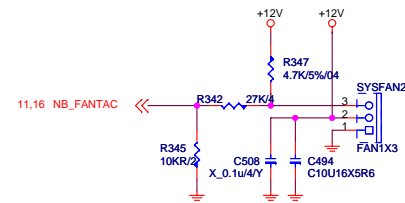
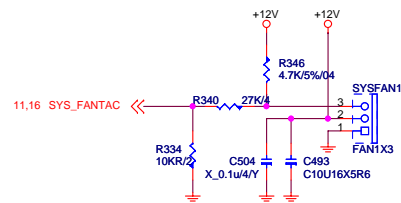
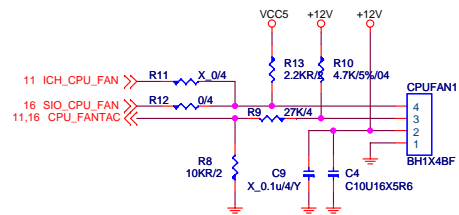


CONN-SATA10P_PURPLE



CONN-SATA10P_PURPLE

FAN-COUNTROL CIRCUIT

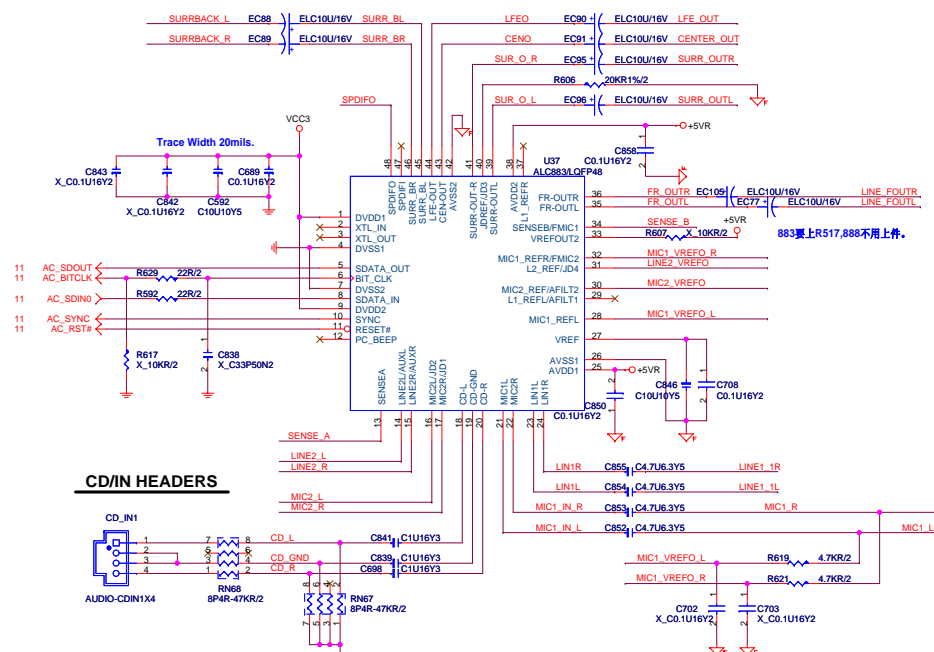


MICRO-STAR INT'L CO.,LTD

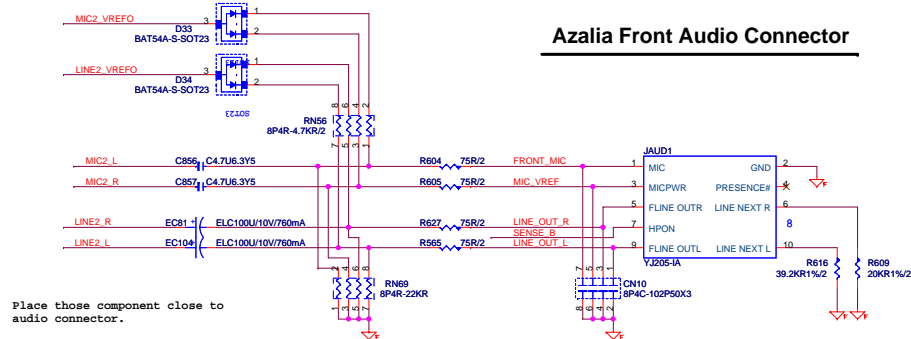
MS-7360

Size	Document Description	Rev
Custom	SATA & e-SATA Ports and Fan Control	1.0
Date:	Tuesday, March 06, 2007	Sheet 18 of 34

ALC888 CODEC

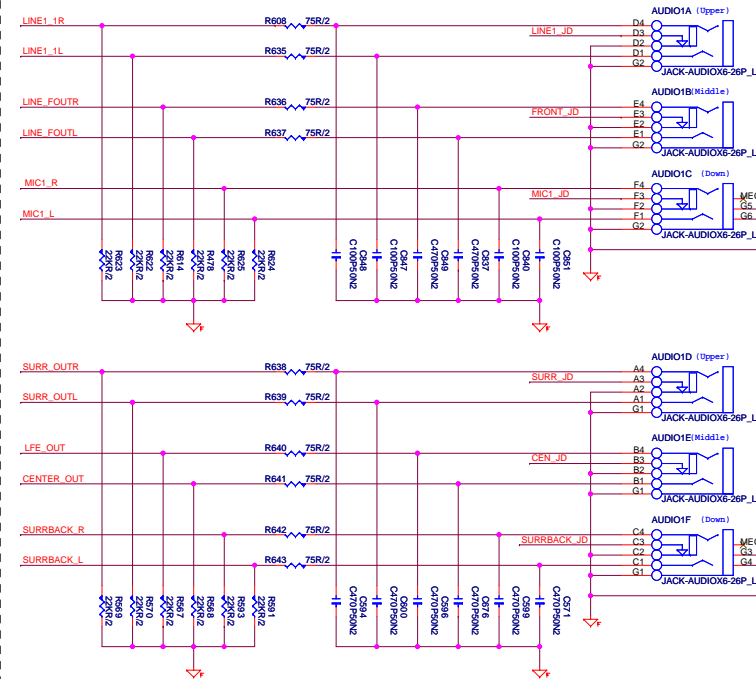


Azalia Front Audio Connector

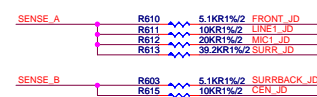


Place those component close to
audio connector.

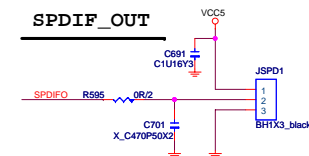
ALC883 JACK



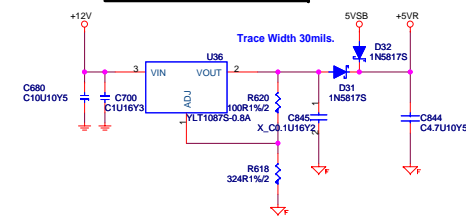
ALC883 JACK DETECT



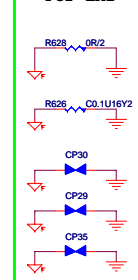
SPDIF_OUT



AUDIO CODE REGULATORS



For EMI



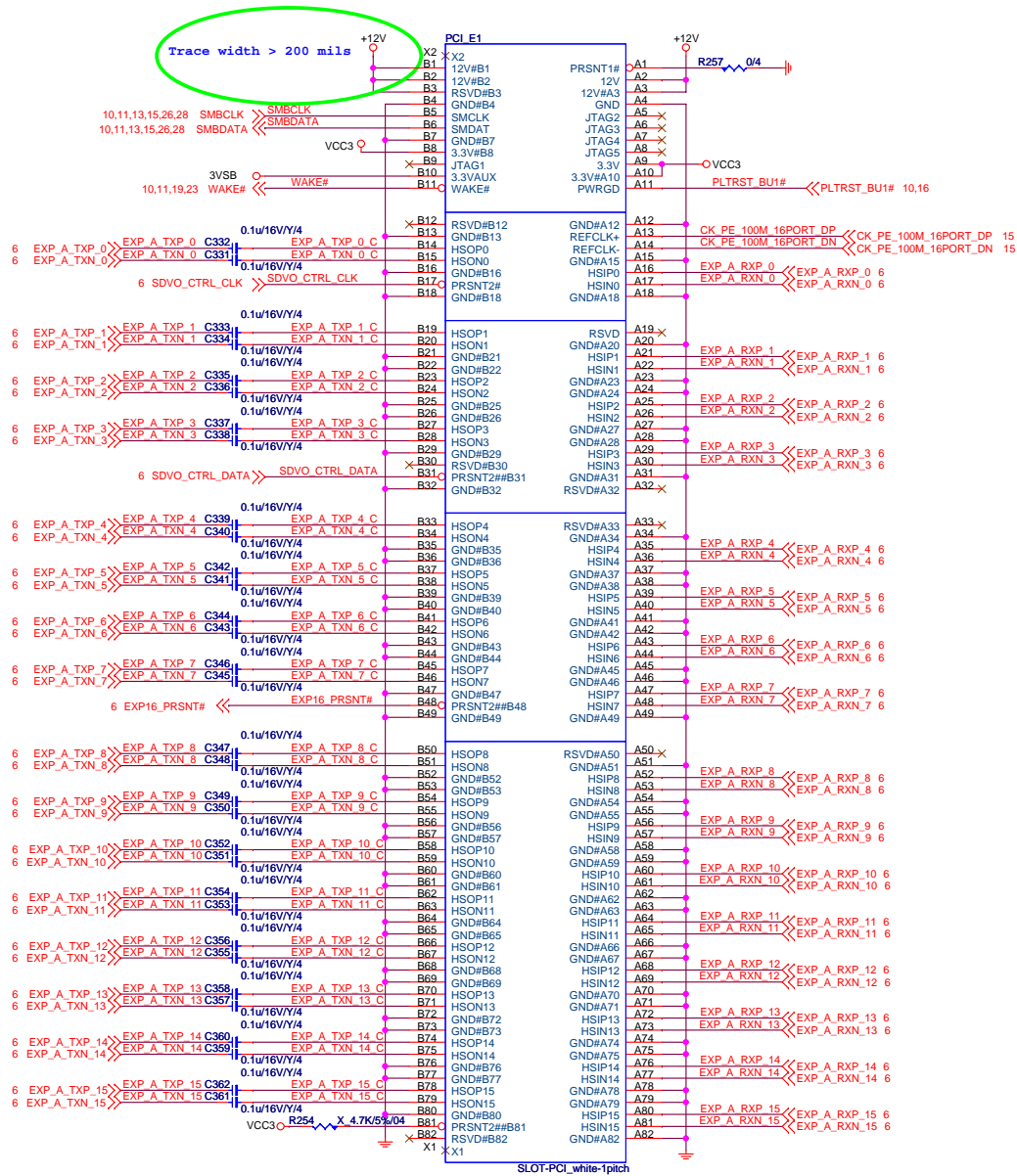
MICRO-STAR INT'L CO.,LTD

MS-7360

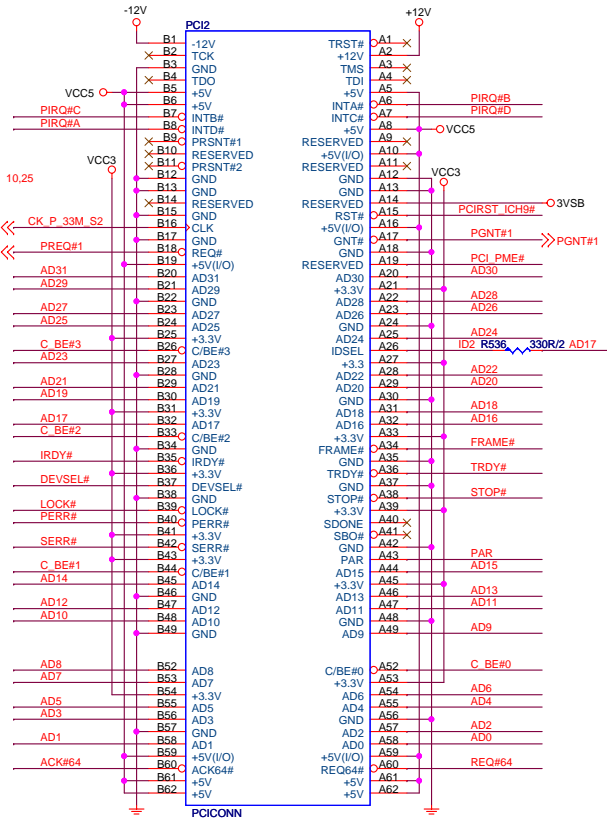
Size Custom	Document Description PCIE_LAN_RTL8111B	Rev 1.0
Date: Monday, March 05, 2007		Sheet 20 of 34



PCI_Express X16 Slot

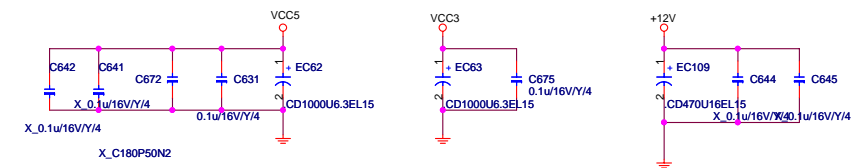


PCI SLOT 2 (PCI VER: 2.2 COMPLY)



10,25 C_BE#[3..0] << C_BE#[3..0]

PCI SLOT DECOUPLING CAPACITORS

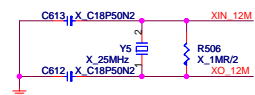
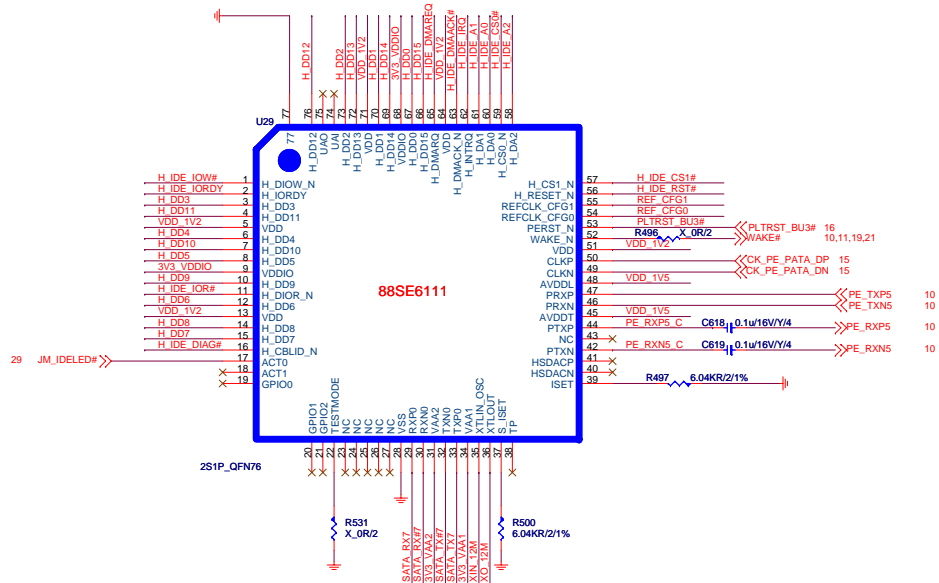


MS-7360

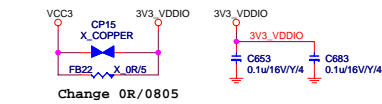
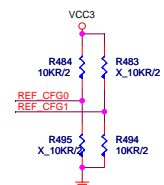
Rev
1.0

Sheet 22 of 34

Hi-Speed PCIE to SATA/PATA Bridge

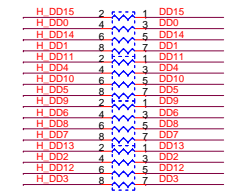
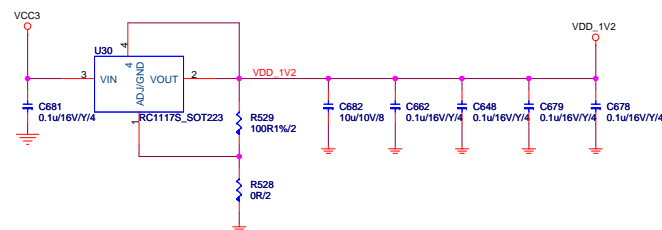
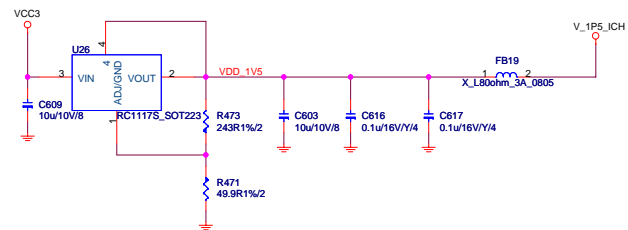
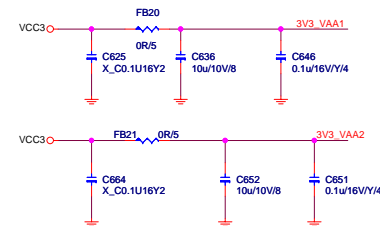


```
REF_CFG[1:0] =  
00:20MHz  
01:25MHz
```

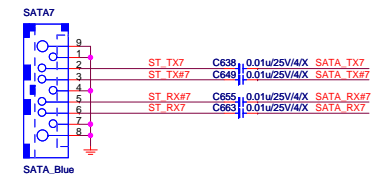
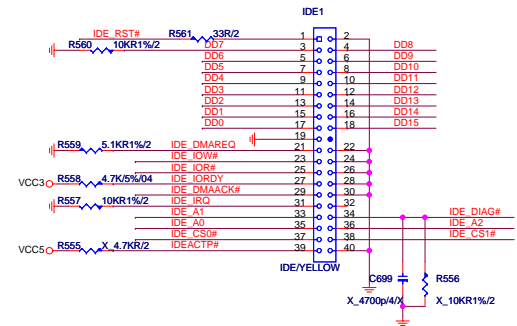


Change 0R/0805

L02-8008074-J07 FOR BEAD



RN60	8P4R-33R/2
RN64	8P4R-33R/2
RN65	8P4R-33R/2
RN62	8P4R-33R/2



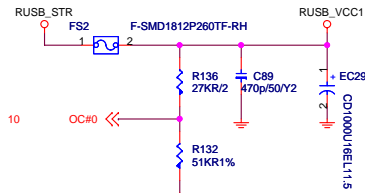
MICRO-STAR INT'L CO.,LTD

MS-7360

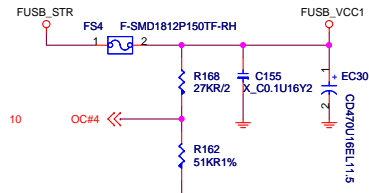
Size Custom	Document Description Marvell 88SE6111 PCIE to PATA/SATA	Rev 1.0
Date: Thursday, March 08, 2007		Sheet 23 of 34

Rear USB Connector

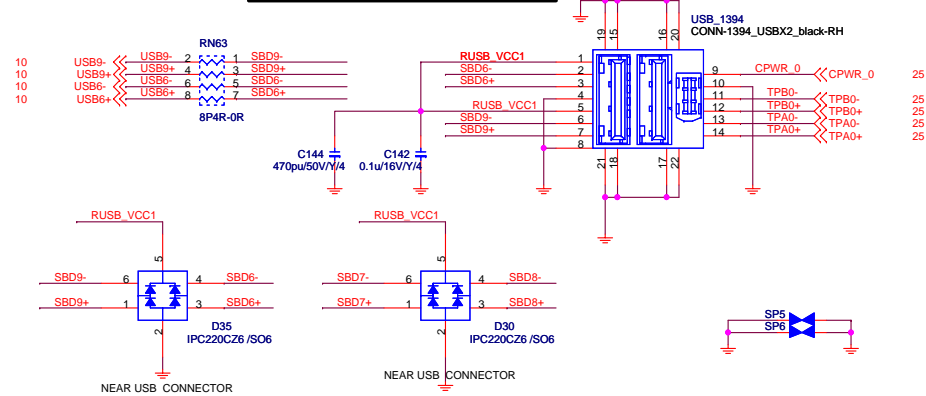
USB POWER FOR PORT 0,1 NEAR CONNECTOR



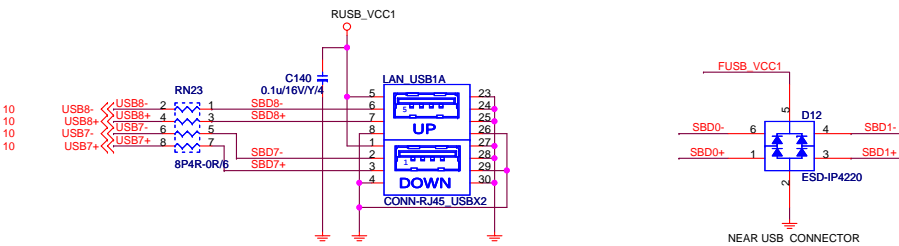
USB POWER FOR PORT 6,7,8,9 NEAR CONNECTOR



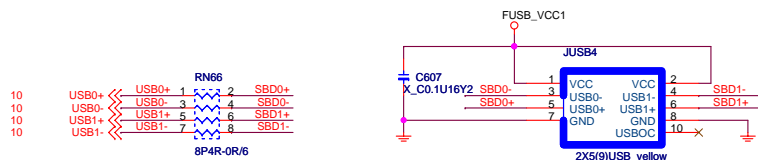
REAR USB PORT 0,1



REAR USB PORT 2,3 (With LAN)

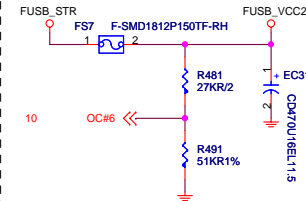


FRONT USB PORT 0,1

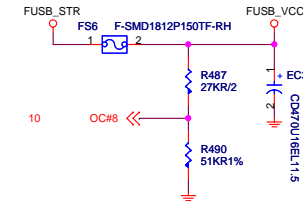


Front USB Connector

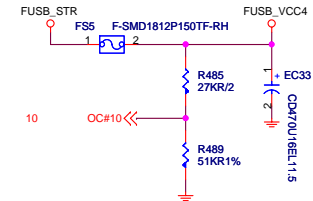
USB POWER FOR PORT 6,7 NEAR CONNECTOR



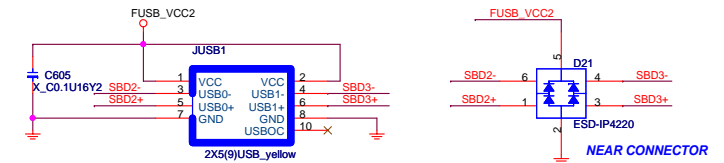
USB POWER FOR PORT 6,7 NEAR CONNECTOR



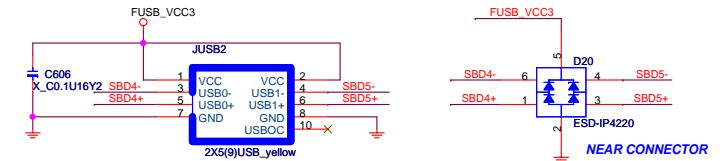
USB POWER FOR PORT 6,7 NEAR CONNECTOR



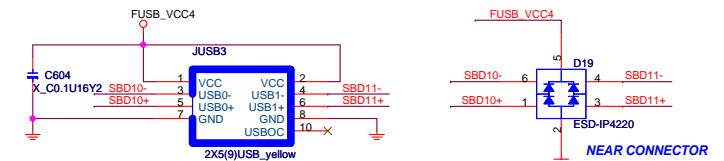
FRONT USB PORT 2,3



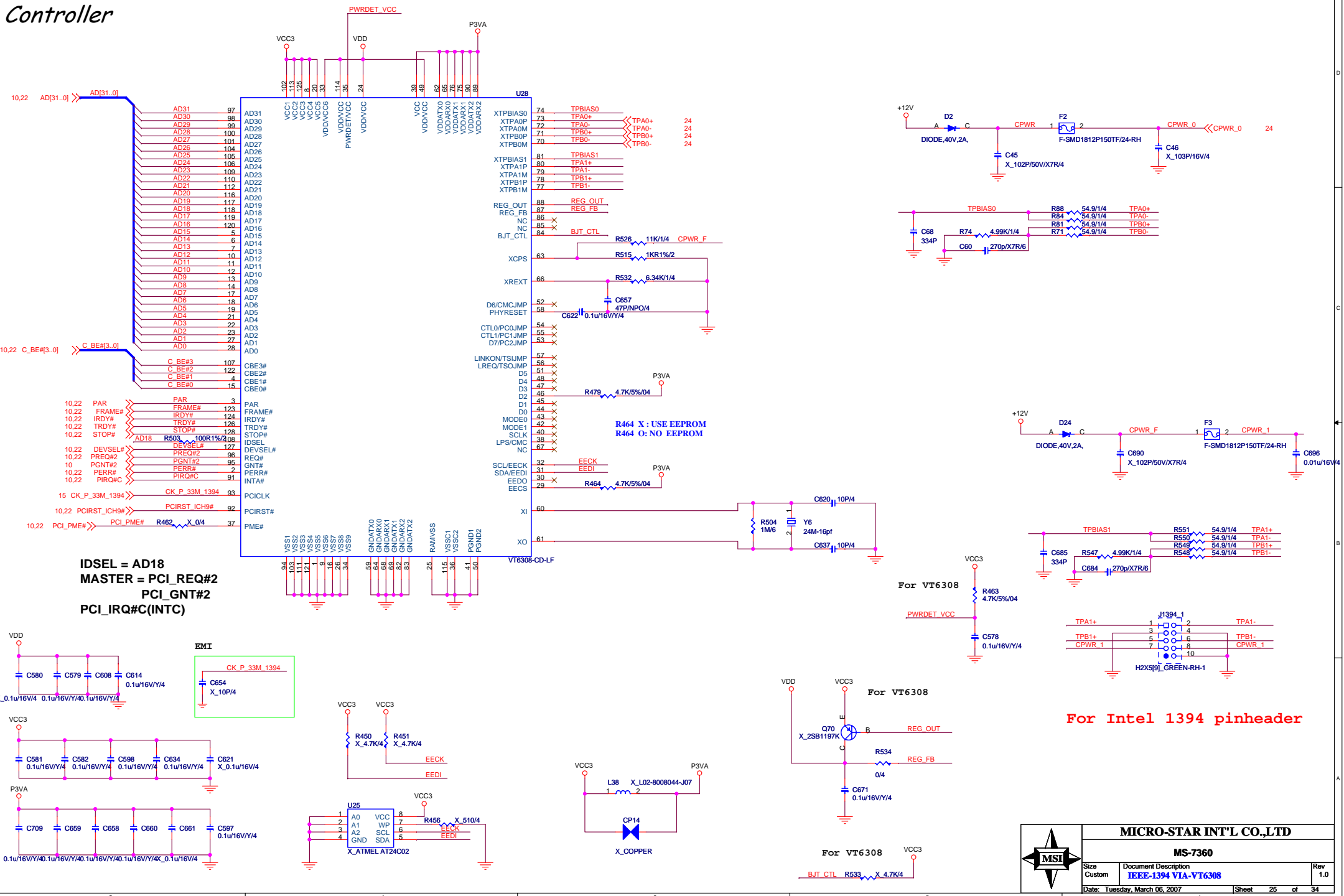
FRONT USB PORT 4,5



FRONT USB PORT 10,11



1394a OHCI Link Layer Controller



The image displays a PCB layout for decoupling capacitors, organized into three main sections: Channel B, Channel A, and EMI. Each section shows the placement of capacitors relative to power and ground planes, with specific component values and footprints labeled.

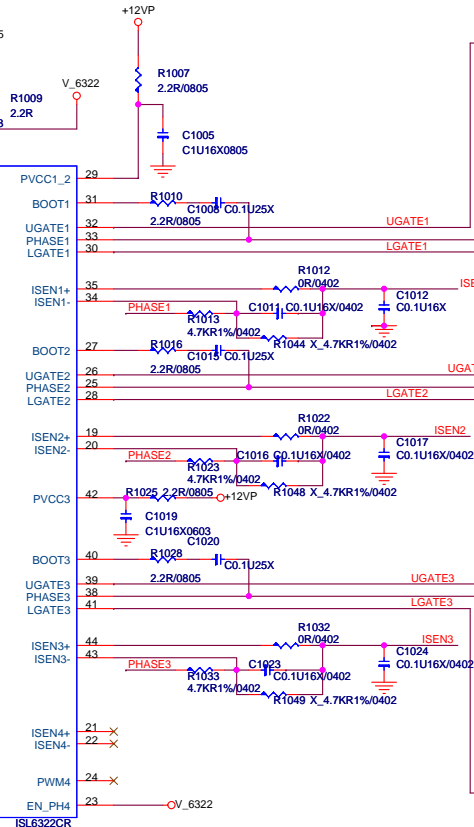
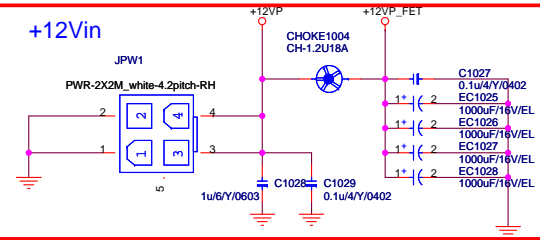
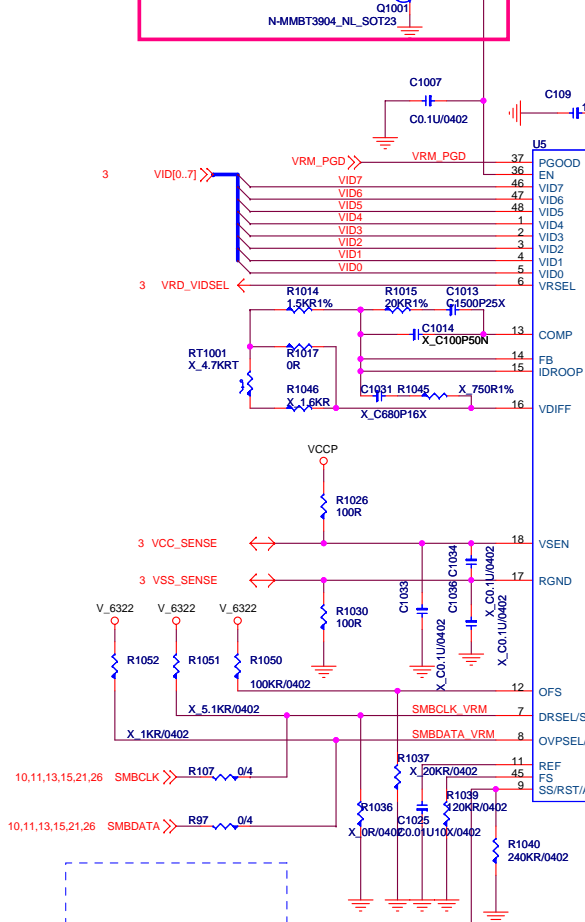
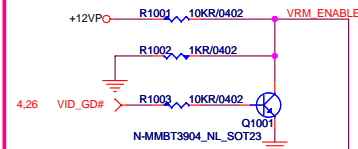
Channel B V_SM_VTT DECOUPLING CAPS: This section shows capacitors C194 through C216, including 180pF and 100pF values, connected to VCC_DDR and VTT_DDR planes.

Channel A V_SM_VTT DECOUPLING CAPS: This section shows capacitors C141 through C150, including 180pF and 100pF values, connected to VCC_DDR and VTT_DDR planes.

For EMI: This section shows capacitors C114 through C117, including 180pF and 100pF values, connected to VCC_DDR and VTT_DDR planes.

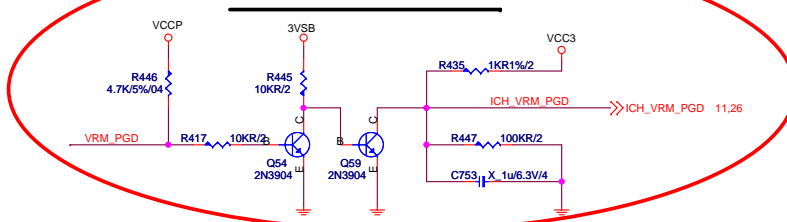
The layout also includes a title block for Micro-Star Int'l Co., Ltd. with the part number MS-7360, a date of Monday, March 05, 2007, and a sheet number of 27 of 34.

VRM_ENABLE

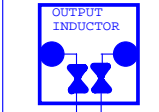
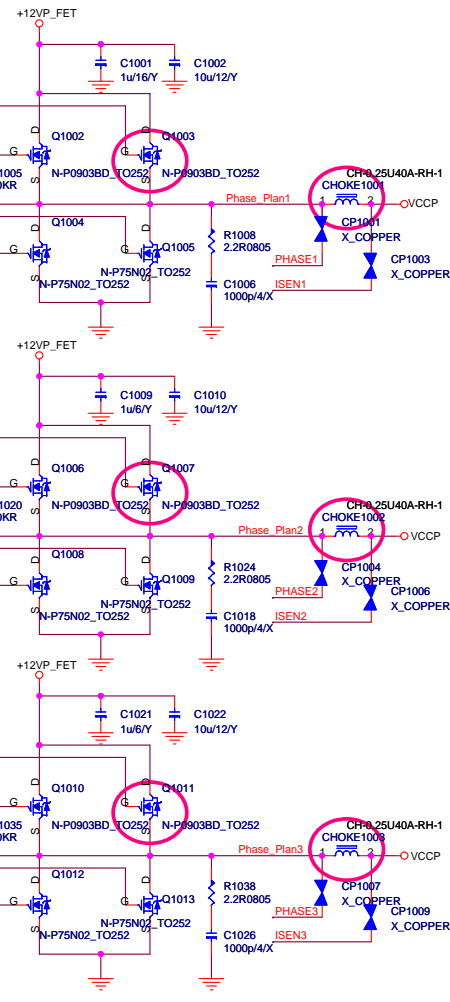


BOTTOM PAD CONNECT TO GND Through 8 VIAs

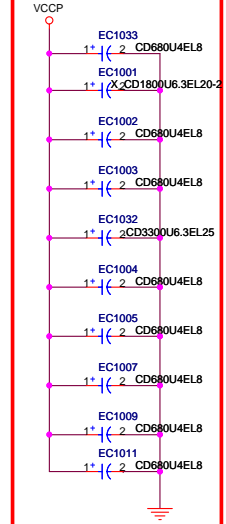
VRMPWRGD LEVEL SHIFT



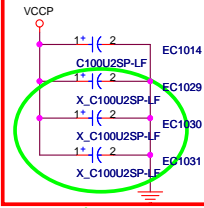
For Intel DG VRM must need level shift



EL-CAP



SP-CAP



Place in bottom

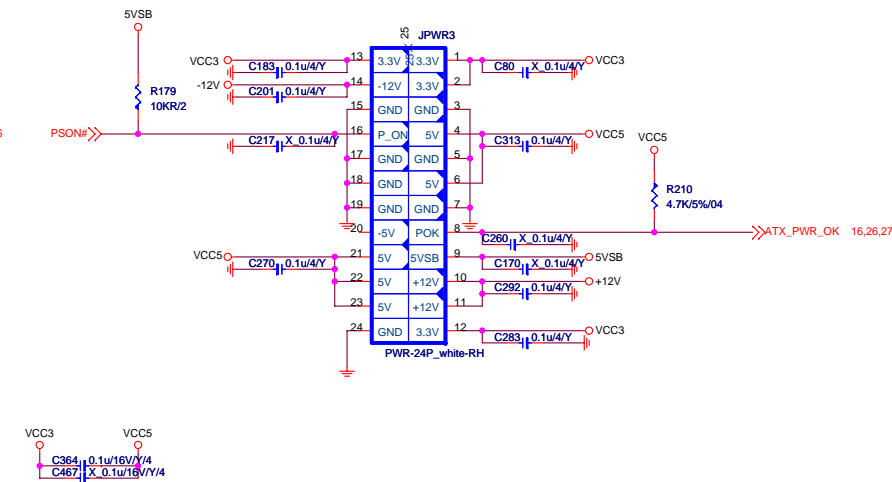


MICRO-STAR INT'L CO.,LTD

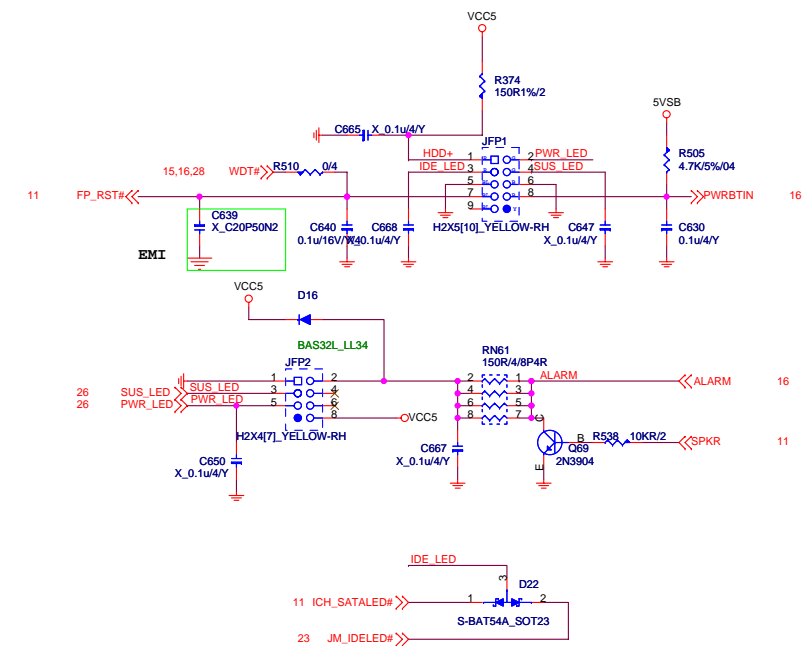
MS-7360

Size	Document Description	Rev
Custom	NB Core Power & DDR Power	1.0
Date: Monday, March 05, 2007	Sheet 28 of 34	

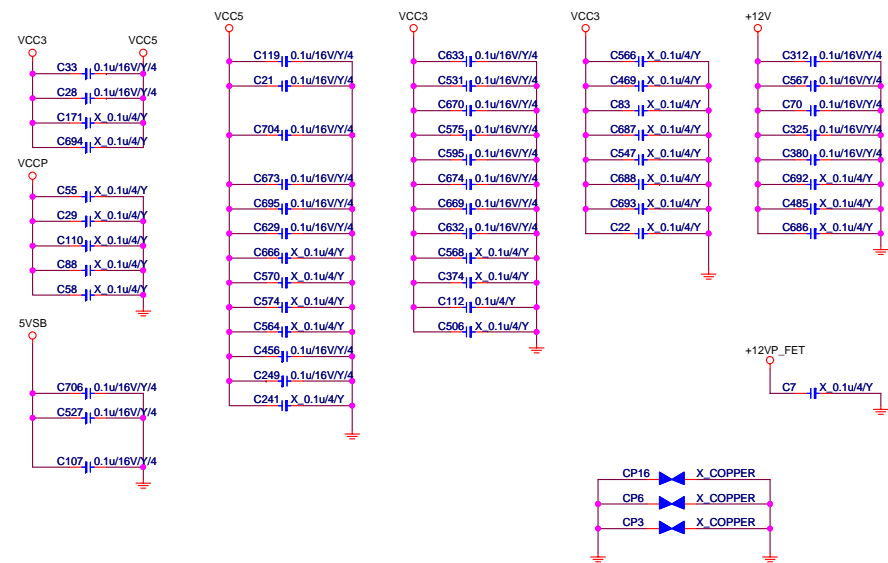
ATX POWER CONNECTOR




FRONT PANNEL



Cap. for EMI & Power





MICRO-STAR INT'L CO.,LTD

MS-7360

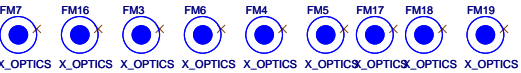
Size Custom Document Description
ATX PWR-Connector & Front Panel

Date: Monday, March 05, 2007 Sheet 29 of 34

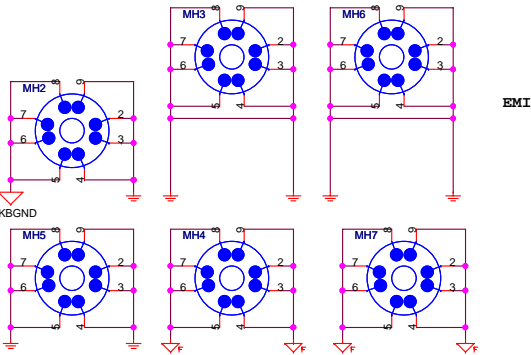
Optical Fiducial Marks-120



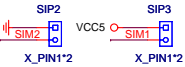
Optical Fiducial Marks-100



Mounting Holes

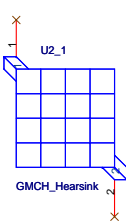


Simulation



7360

P80-073600A-D05, 縹 () 縹 嘲, 23, 縹 縹幅紅
P80-0736050A-Y34, 縹 縹, 23, 縹 縹幅紅



LGA775-CPU		
0.8375V - 1.6000V Core	-	125A
1.2V FSB Vtt	-	4.6A

Bearlake-G (G33)		
1.2V FSB_VTT	-	1.2 A
1.25V Core	-	13.8A
1.25V DMI/PCI Exp.	-	2.47 A
1.5V VCC_DDR	-	3.3A
1.5V VCC_SMCLK	-	350mA
3.3V VCCA_DAC	-	66 mA
3.3V VCC33	-	15.8mA
1.25V Vcc CL	-	4.9A

ICH9		
1.05V Core	-	1.16A
1.25V DMI	-	41 mA
1.2V FSB_VTT	-	2 mA
1.5V_A USB/SATA/PLL	-	1.65A
1.5V_B PCI Exp.	-	0.65A
VCCRTC	-	6 uA
3.3V CL	-	19 mA
1.5V GbE LAN	-	87 mA
3.3V VccSus3_3	-	200mA
3.3V Vcc3_3	-	308mA
3.3V 10/100 LAN	-	19 mA
3.3V GbE LAN	-	1 mA
3.3V HDA	-	32 mA
3.3V SusHDA	-	33 mA

1394 Controller VT6308		
3.3V	-	156mA

HD Audio STAC9227		
3.3V AUDIO	-	32mA
5V AUDIO	-	200mA

CK505		
3.3V VDD_48/PCI/REF	-	250mA
0.3V - 1V CPU/SRC/DOT/PLL	-	80mA

RTL8111B		
3.3V_SB I/O & LED	-	668mA
1.8V EVDD/AVDD	-	198mA
1.5V VDD	-	367mA

ISL6306		
VCCP VRD11/10.x	-	0.8375V-1.6000V
4-Phase Switch	-	

W83310DS		
VTT_DDR	-	0.75V Linear 0.83A

uP6103 SW-Power		
VCC_DDR	-	1.5V PWM 18.64A

uP6103 SW-Power		
V_1P25_CORE	-	1.25V PWM 21.21A

MS12 Controller		
V_1P05_ICH	-	1.05V Linear 1.16A
V_FSB_VTT	-	1.2V Linear 5.8A
V_1P5_ICH (TO263)	-	1.5V Linear 2.31A
VCC3_SB	-	3.3V Linear 2.5A
5VDUAL1	-	5V Switch 6.35A
5VDIMM	-	5V Switch 6.99A

DDRIII x4 & TERMINATOR		
0.9V VTT_DDR	-	0.83A
1.5V VCC_DDR (S0,S1)	-	7.2A

PCI Express x16 slot		
+12V	-	5.5 A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

PCI Express x 1 slot		
+12V	-	0.5 A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

PCI Express x 4 slot		
+12V	-	5.5A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

PCI slot x2		
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	7.6A
+5V	-	5.0A
+12V	-	0.5A

USB x12		
+5V (S0,S1)	-	6.0A
+5V (S3)	-	20mA

PS2		
+5V (S0,S1)	-	345mA
+5V (S3)	-	2.0mA

5VAudio		
+5VR	-	500mA

+12V		
ATX 2x2	-	

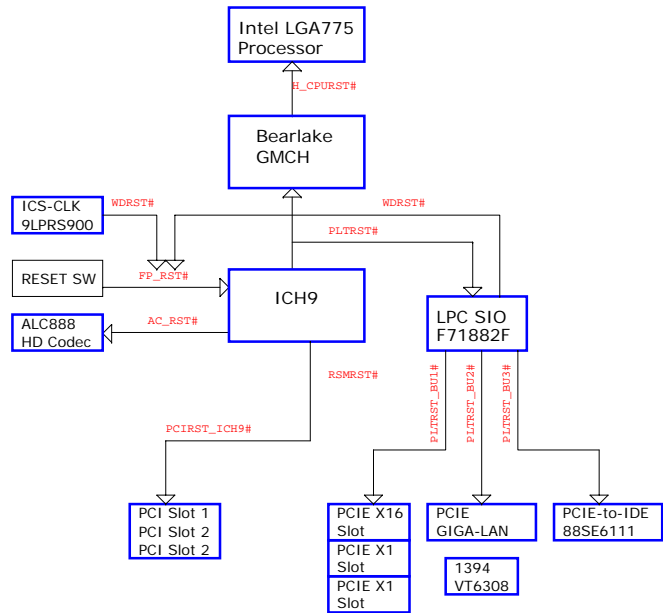
ATX POWER			
+5V	+3.3V	+5VSB	+12V

■ Bead or Inductor
 X-Copper

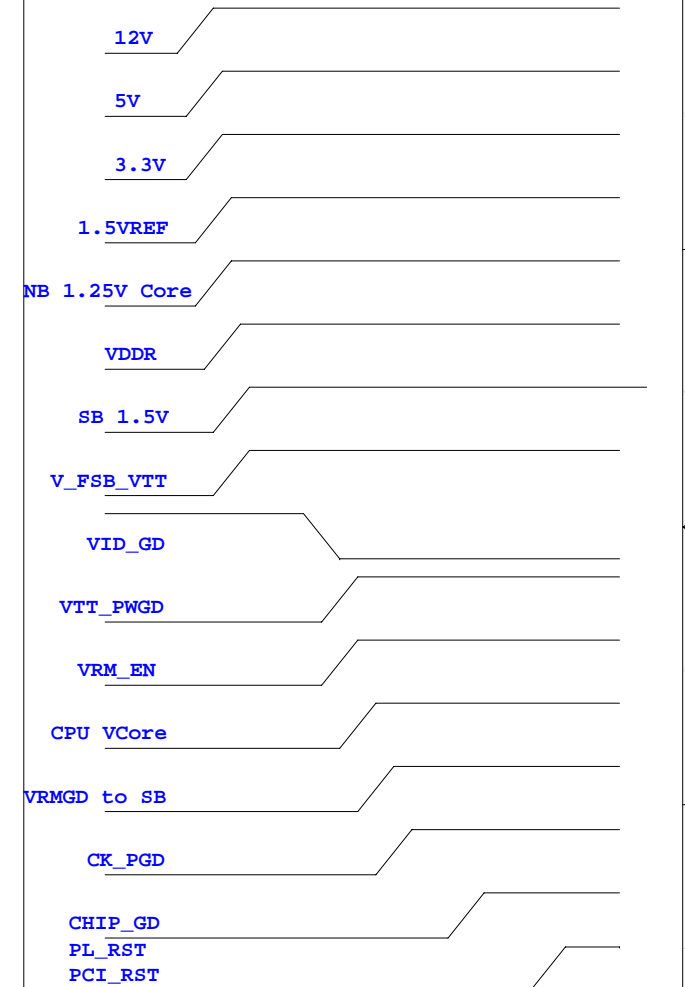
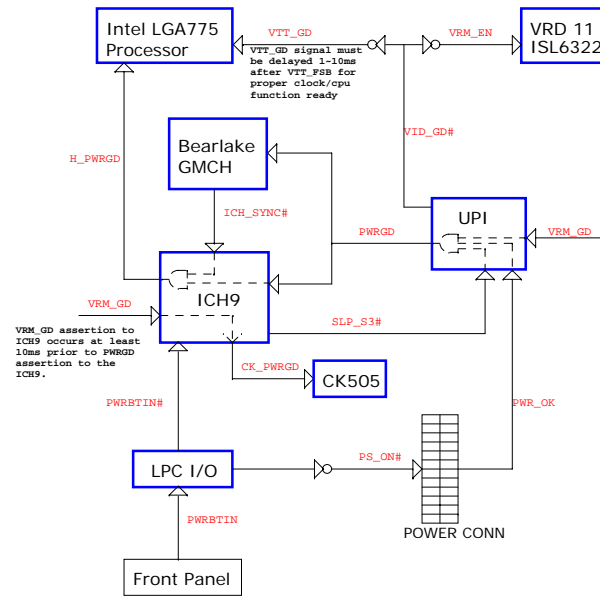


MICRO-STAR INT'L CO.,LTD			
MS-7360			
Size Custom	Document Description Power Delivery	Rev 1.0	
Date: Monday, March 05, 2007	Sheet 31	of 34	

RESET MAP



PWROK MAP



ICH8

GPIO	Alt Func	I/O/NC	Power	ToI	Default	Signal Name
GPIO[0]	BM_BUSY#	I/O	Core	3.3V	GPI	
GPIO[1]	TACH1	I/O	Core	3.3V	GPI	SYS1_FANTAC
GPIO[5:2]	PIRQ[H:E]#	I/OD	Core	5V	GPI	PIRQ#[H:E]
GPIO[7:6]	TACH[3:2]	I/O	Core	3.3V	GPI	SYS2/3_FANTAC
GPIO[8]	unmuxed	I/O	Resume	3.3V	GPI	
GPIO[9]	WOL_EN	I/O	Resume	3.3V	Native	
GPIO[10]	CLGPIO1	I/O	Resume	3.3V	GPI	
GPIO[11]	SMBALERT#	I/O	Resume	3.3V	Native	
GPIO[12]	unmuxed	I/O	Resume	3.3V	GPO	
GPIO[13]	unmuxed	I/O	Resume	3.3V	GPI	SIO_PME#
GPIO[14]	CLGPIO2	I/O	Resume	3.3V	GPI	
GPIO[15]	unmuxed	I/O	Resume	3.3V	Native	
GPIO[16]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[17]	TACH0	I/O	Core	3.3V	GPI	CPU_FANTAC
GPIO[18]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[19]	SATA1GP	I/O	Core	3.3V	GPI	
GPIO[20]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[21]	SATA0GP	I/O	Core	3.3V	GPI	
GPIO[22]	SCLOCK	I/O	Core	3.3V	GPI	
GPIO[23]	LDRQ1#	I/O	Core	3.3V	Native	
GPIO[24]	CLGPIO0	I/O	Resume	3.3V	GPO	
GPIO[25]	STP_CPU#	I/O	Resume	3.3V	Native	
GPIO[26]	S4_STATE#	I/O	Resume	3.3V	Native	
GPIO[27]	QRT_STATE0	I/O	Resume	3.3V	GPO	
GPIO[28]	QRT_STATE1	I/O	Resume	3.3V	GPO	
GPIO[29]	OC5#	I/O	Resume	3.3V	Native	OC#4
GPIO[30]	OC6#	I/O	Resume	3.3V	Native	OC#6
GPIO[31]	OC7#	I/O	Resume	3.3V	Native	OC#6
GPIO[32]	unmuxed	I/O	Core	3.3V	GPO	SPI_WP#
GPIO[33]	unmuxed	I/O	Core	3.3V	GPO	SPI_HOLD_GPO#
GPIO[34]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[35]	SATACLKREQ#	I/O	Core	3.3V	GPO	
GPIO[36]	SATA2GP	I/O	Core	3.3V	GPI	
GPIO[37]	SATA3GP	I/O	Core	3.3V	GPI	
GPIO[38]	SLOAD	I/O	Core	3.3V	GPI	
GPIO[39]	SDATAOUT0	I/O	Core	3.3V	GPI	
GPIO[43:40]	OC[4:1]#	I/O	Resume	3.3V	Native	OC#0;OC#4
GPIO[47:44]	OC[11:8]#	I/O	Resume	3.3V	Native	OC#8;OC#10
GPIO[48]	SDATAOUT1	I/O	Core	3.3V	GPI	
GPIO[49]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[50]	REQ1#	I/O	Core	5V	Native	PREQ1#
GPIO[51]	GNT1#	I/O	Core	3.3V	Native	PGNT1#
GPIO[52]	REQ2#	I/O	Core	5V	Native	PREQ2#
GPIO[53]	GNT2#	I/O	Core	3.3V	Native	PGNT2#
GPIO[54]	REQ3#	I/O	Core	5V	Native	PREQ3#
GPIO[55]	GNT3#	I/O	Core	3.3V	Native	PGNT3#
GPIO[56]	GLAN_DOCK#	I/O	Resume	3.3V	GPI	
GPIO[57]	CLGPIO5	I/O	Resume	3.3V	GPI	
GPIO[58]	SPI_CS1#	I/O	Resume	3.3V	GPI	SPI_CS1#
GPIO[59]	OC#0	I/O	Resume	3.3V	Native	OC#0
GPIO[60]	LINKALERT#	I/O	Resume	3.3V	Native	

JUMPER SETTING

JBAT1	(1-2)NORMAL	(2-3)CLEAR
-------	-------------	------------

SIO(F71882)

PIN NAME	USAGE	Input/Output	NOTES
GPIO[2:0]	MCH_BSEL2:0]	OUTPUT	PROGRAMED BSEL[2:0] OUTPUT
GPIO3	PCIEX1#	OUTPUT	PROGRAMED X1/X4 OPTION OUTPUT
GPIO4	UNUSED		
GPIO5	UNUSED		
GPIO6	UNUSED		
GPIO7	WDT#	OUTPUT	WATCH DOG TIMER RESET OUTPUT
GPIO10	DLED1	OUTPUT	DEBUG LED OUTPUT 1
GPIO11	UNUSED		
GPIO12	UNUSED		
GPIO13	BEEP	OUTPUT	
GPIO14	UNUSED		
GPIO15	DLED2	OUTPUT	DEBUG LED OUTPUT 2
GPIO16	DLED3	OUTPUT	DEBUG LED OUTPUT 3
GPIO17	UNUSED		
GPIO20	PLTRST_BU#1	OUTPUT	PCI RESTE BUFFER1
GPIO21	PLTRST_BU#2	OUTPUT	PCI RESTE BUFFER2
GPIO22	PLTRST_BU#3	OUTPUT	PCI RESTE BUFFER3
GPIO23	UNUSED		
GPIO24	PWR_OK	INPUT	ATX POWER OK INPUT
GPIO26	PWRBTIN	INPUT	FRONT PANNEL POWER BUTTON
GPIO27	PWRBTN#	OUTPUT	POWER BUTTON BUFFER OUT
GPIO30	SLP_S3#	INPUT	FRONT SOUTBRIDGE S3#
GPIO31	PSON#	OUTPUT	OUTPUT FOR ATX POWER ON
GPIO32	DLED4	OUTPUT	DEBUG LED OUTPUT 4
GPIO33	UNUSED		
GPIO40	SYS2_FANTAC	INPUT	
GPIO41	UNUSED		
GPIO42	IRTX	OUTPUT	
GPIO43	IRRX	INPUT	
VIDIN[2:0]	CPU_BSEL[2:0]	INPUT	CPU BSEL[2:0] INPUT
VIDIN3	UNUSED	INPUT	RESERVED FOR PCIE X4 INDICATION

DDR-III DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	00	P/N_DDR0_A P/N_DDR2_A
DIMM 2	01	P/N_DDR3_A P/N_DDR5_A
DIMM 3	10	P/N_DDR0_B P/N_DDR2_B
DIMM 4	11	P/N_DDR3_B P/N_DDR4_B

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	CK_P_33M_S1
PCI Slot 2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	CK_P_33M_S2
1394	PIRQ#D	PREQ#2 PGNT#2	AD18	CK_P_33M_1394



MICRO-STAR INT'L CO.,LTD			
MS-7360			
Size Custom	Document Description GPIO setting & PCI Routing		Rev 1.0
Date: Monday, March 05, 2007		Sheet 33 of 34	

- HW Ver.0A Change to Ver.0B List:
- 1.Remove Q54 and R374and short Q54 B,C pin for power sequence.(page26)
 - 2.U24 power change from VCC3 to 3VSB for power sequence.(page26)
 - 3.Change EC42 from 470u to 820u for V_FSB_VTT power noise.(page26)
 - 4.Change EC52 from 470u to 820u for SB1_05 power noise.(page26)
 - 5.Change EC53 from 470u to 820u for SB1_5 power noise.(page26)
 - 6.CPU_GTLREF resistor value R119 , R115, R128, R104 change from 50ohm to 100ohm for pull-up(intel suggestion)(page4)
 - 6.CPU_GTLREF resistor value R124 , R117 , R141 , R105 change from 100ohm to 200ohm for pull-down.(intel suggestion)(page4)
 - 7.MCH_GTLREF resistor value R190 change from 50ohm to 100ohm for pull-pu.(intel suggestion)(page6)
 - 8.MCH_GTLREF resistor value R195 change from 100ohm to 200ohm for pull-down.(intel suggestion)(page6)
 - 9.SRCOMP[3:0] R223 , R227 , R184 , R182 change from 20ohm to 19.1ohm.(intel suggestion)(page7)
 - 10.DDR2 termination RN16 , RN26 , RN11 , RN14 , RN27 , RN12 , R171 change from 39ohm to 43ohm.(intel suggestion)(page14)
 - 11.Add CK_DOT96_MCH_DP pull-high 1.25V and CK_DOT96_MCH_DN pull-down for non-graphic SKU.(intel suggestion)(page6)
 - 12.RIRQ[H:A] pull-up 2.7Kohm to VCC5.(intel suggestion)(page22)
 - 13.USB have two group [5:0] EHCI#1,[6:11EHCI#2 , please one group to real and one group to front.(intel suggestion)(page24)
 - 14.Audio VREFOUT_E and VREFOUT_F swap.(for schematic error)(page20)
 - 15.Audio BASS and CEN_OUT swap.(for schematic error)(page20)